

# Compal Confidential

## DIS M/B Schematics Document

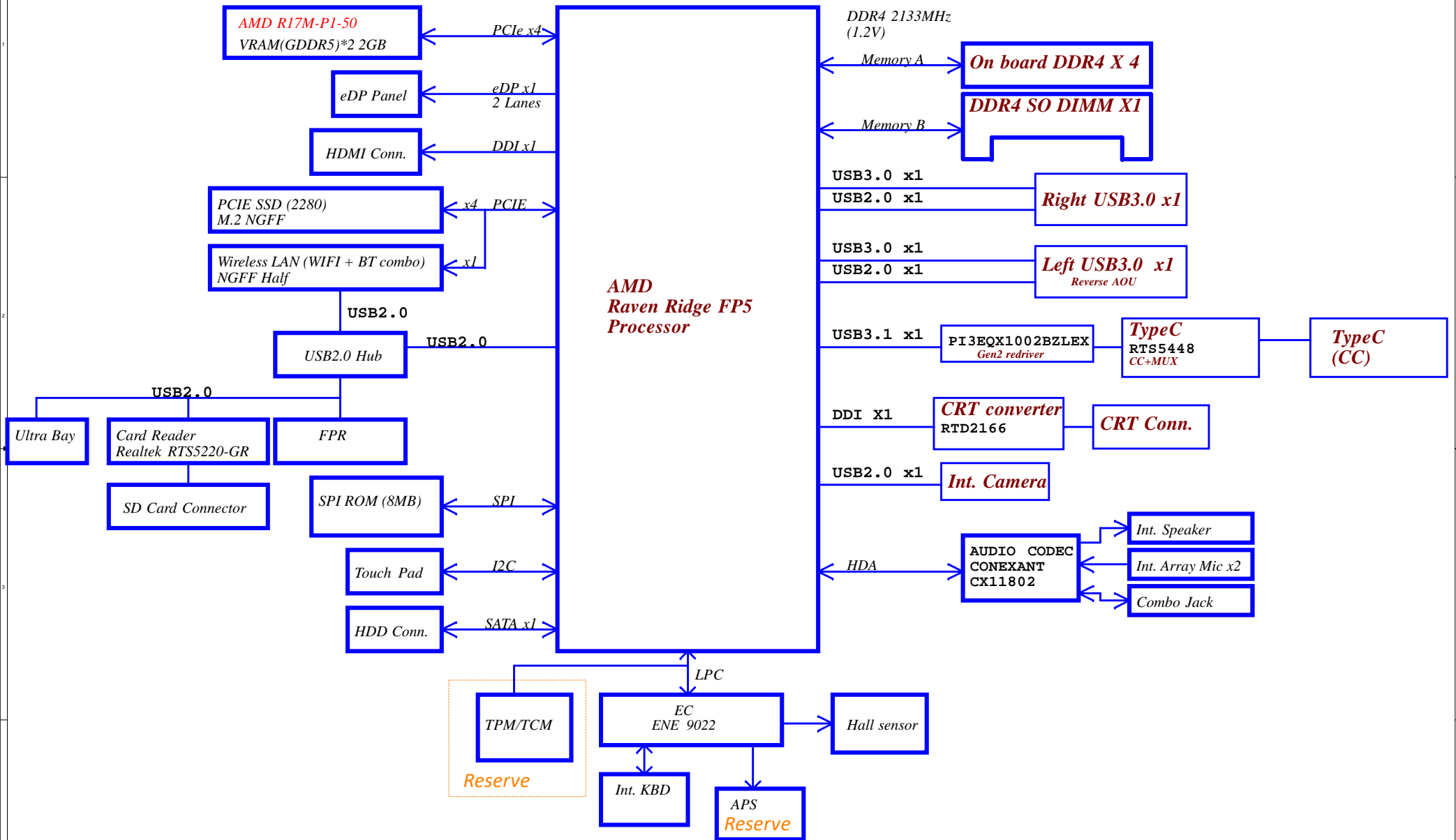
### AMD Raven Ridge FP5 APU with DDR4

### AMD R17M-P1-50

2018-02-01

LA-F485PR10

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## Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.8VALW	0.95V always on power rail	ON	ON	ON
+0.8VS	0.95V switched power rail	ON	OFF	OFF
+1.2V_DDR	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V_MEM	2.5V power rail for DDR	ON	ON	OFF
+0.6VS_VTT	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VS_VRAM	1.35V switched power rail for VGA DDR	ON	OFF	OFF
+VDDCI	0.8V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON

## SMBUS Control Table

	SOURCE	VGA	BATT	EC	SODIMM	WLAN	APU
EC_SMB_CK1 EC_SMB_DA1	9022 +3VALW	X	V +3VALW	V +3VALW	X	X	X
APU_SCLCK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	9022 +3VS	X	X	V +3VALW	X	X	V +1.8VS (+3VS)

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	GPU	0x41/0x41	
Charger	0001 0010 b	12H	APS	3Dh/3Ch	
			VGA Converter	0x64/0x65	

## USB OC MAPPING

OC#	USB Port	
0	USB20_0_port2	
1	USB20_i_port0	
2	USB HUB	
3		

APU SM Bus address			
SM Bus 0	Device	Address	HEX
	DDR DIMM1	1010 001Xb	A2H
APU I2C Bus address			
I2C 3	Device	Address	
	Touch Pad (Synaptics)	\$2C	
	Touch Pad (Elan)	0X15	

## GPP Port Table

Port	Device
GPP0	
GPP1	
GPP2	SSD (PCIE)
GPP3	
GPP4	LAN (PCIE)
GPP5	WLAN (PCIE)
GPP6	HDD (SATA)
GPP7	

## DisplayPort Table

Port	Device
0	eDP
1	HDMI
3	DisplayPort -> CRT
2	

## USB3.0 Port Table

Port	Device	Port	Device
0		0	Camera
1	Type C Right	1	Type C Right
2	USB3.0 Left	2	USB3.0 Left
3	USB3.0 Right	3	USB3.0 Right
4		4	
		5	USB Hub
		5-1	Card Reader
		5-2	BT
		5-3	Ultra Bay
		5-4	FP

## USB2.0 Port Table

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LA-F484P Power Sequence

Boot

Shut  
Down

EC Pin 110 Input

EC Pin 112 Output

AC Plug

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 123 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Output

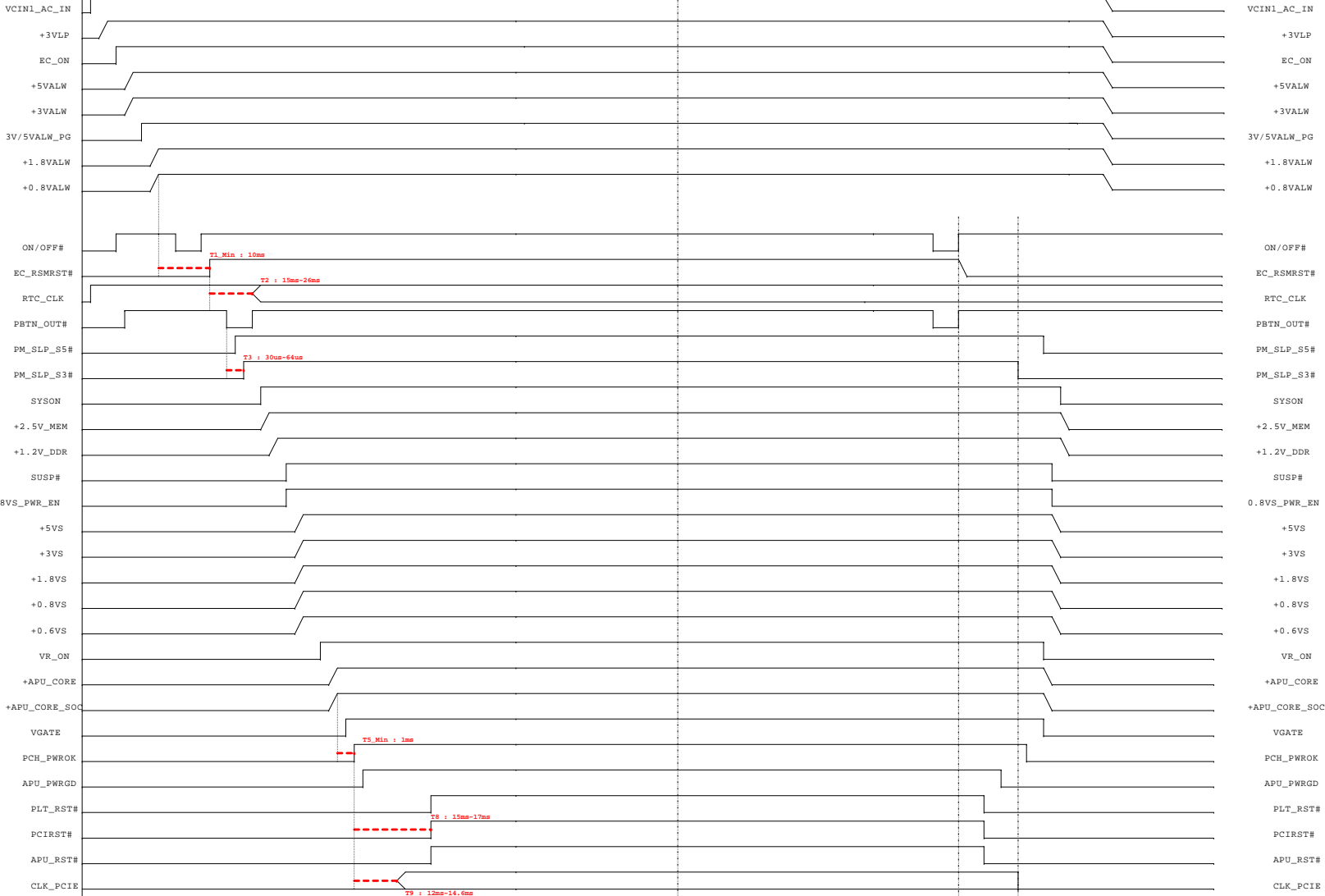
EC Pin 99 Output

EC Pin 121 Output

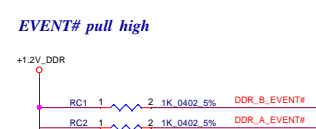
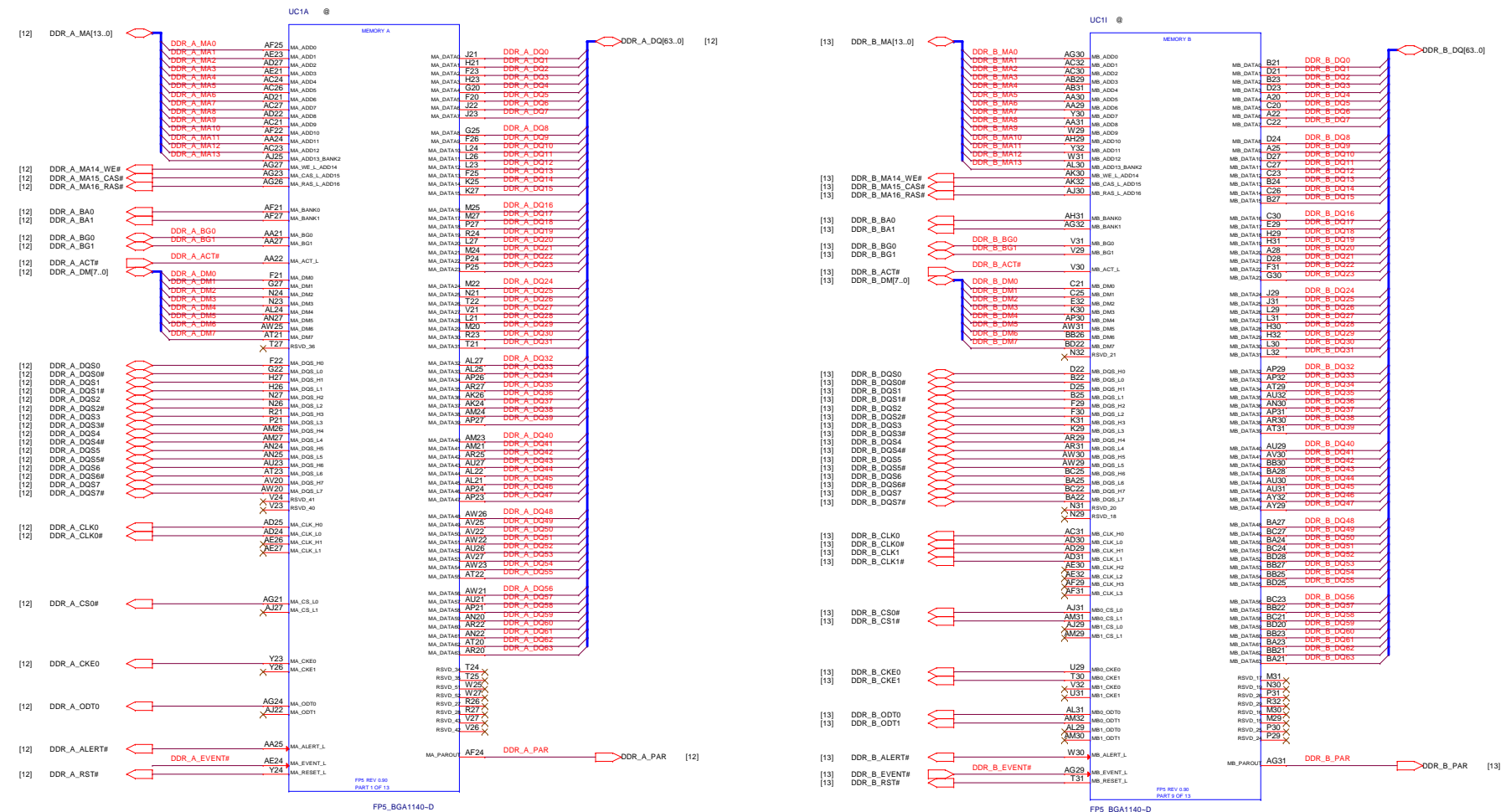
EC Pin 36 Input

EC Pin 32 Output

EC Pin 13 Input

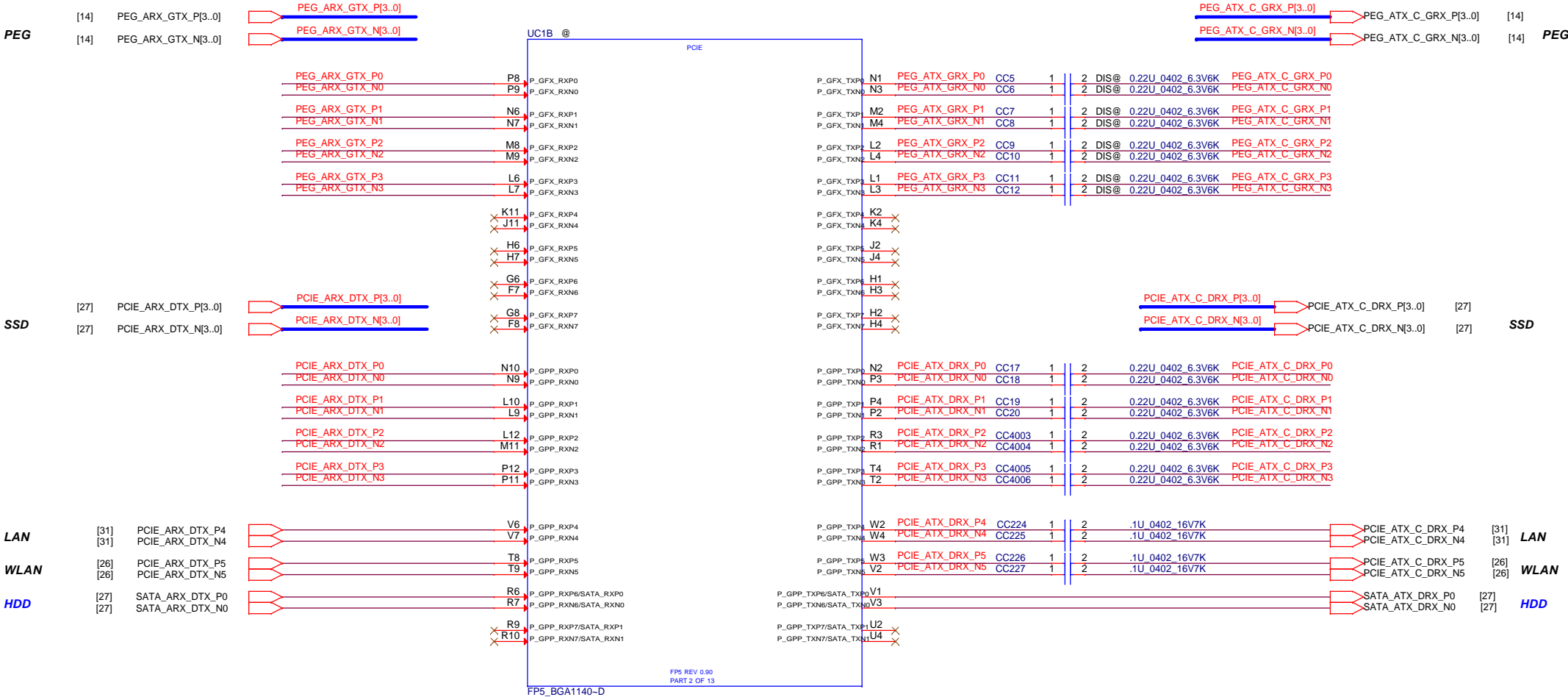


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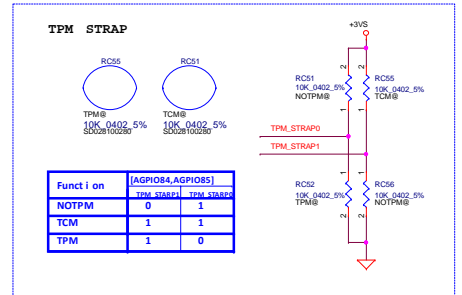
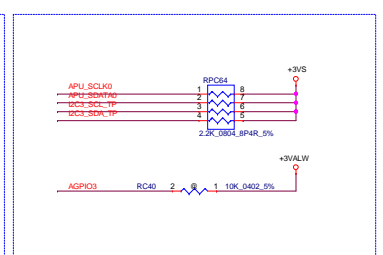
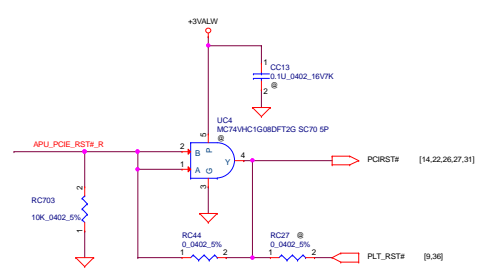
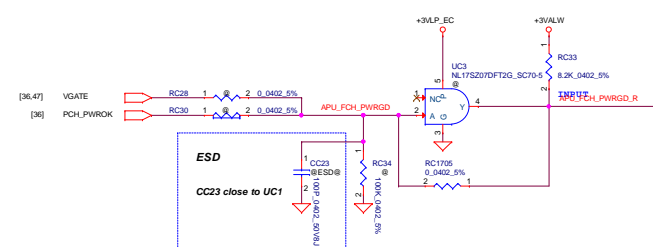
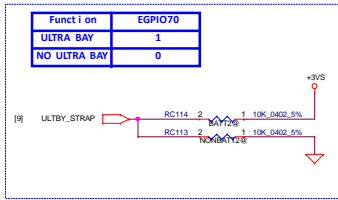
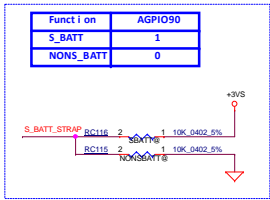
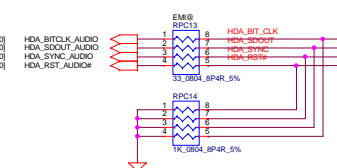
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Main Func = CPU



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Function	[AGPIO84,AGPIO85]	
	TPM_STARP1	TPM_STARP0
NOTPM	0	1
TCM	1	1
TPM	1	0

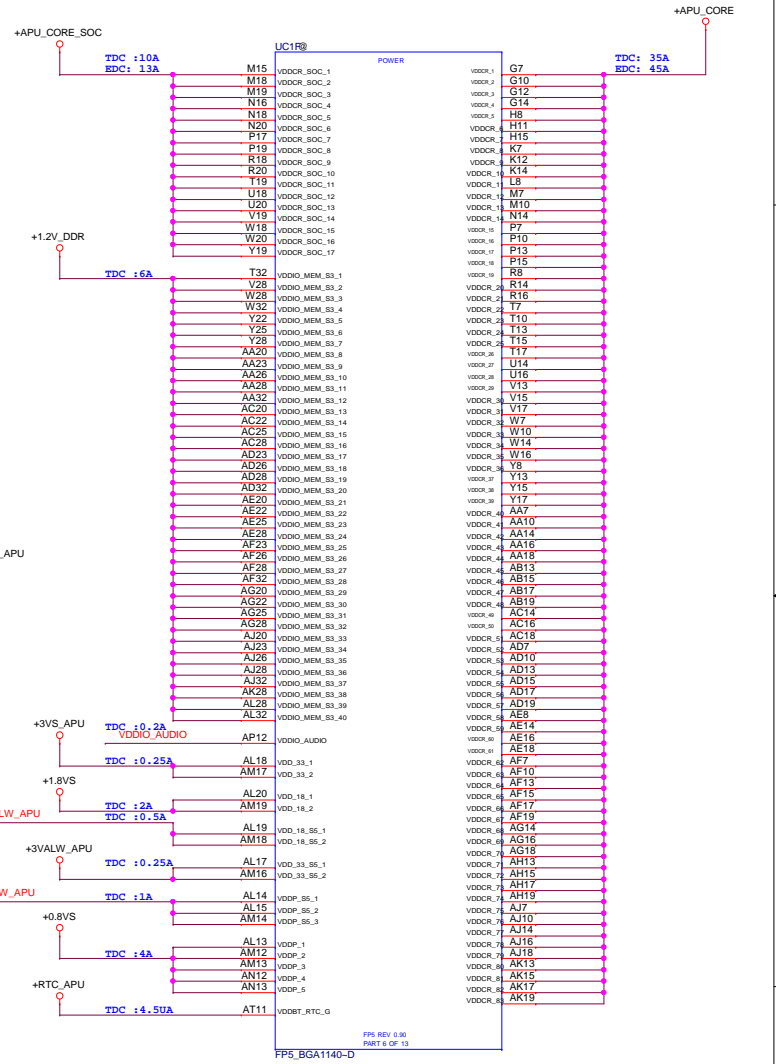
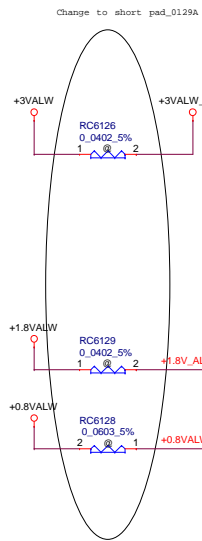
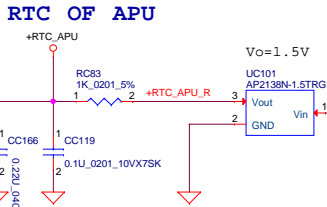
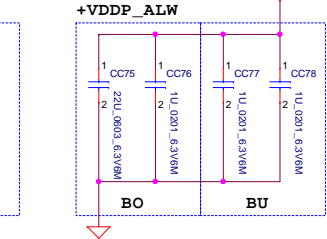
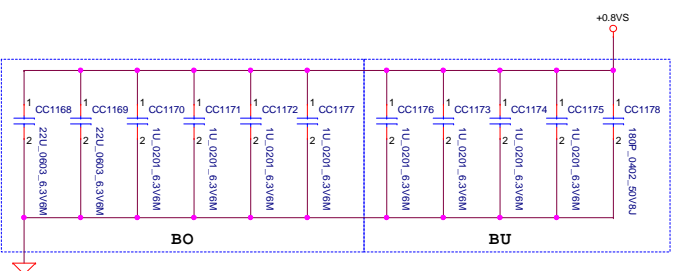
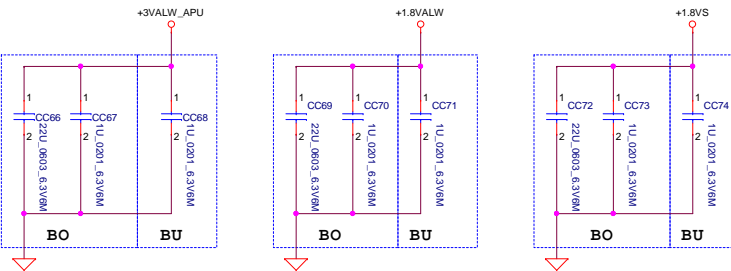
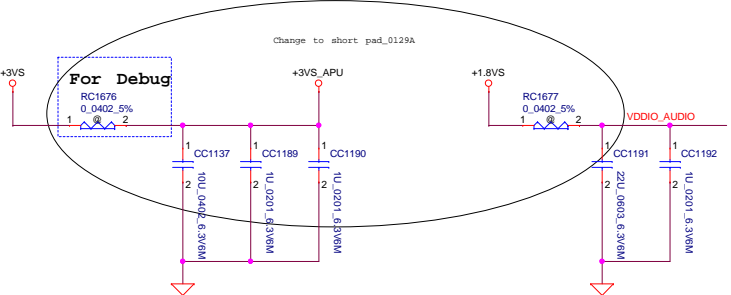
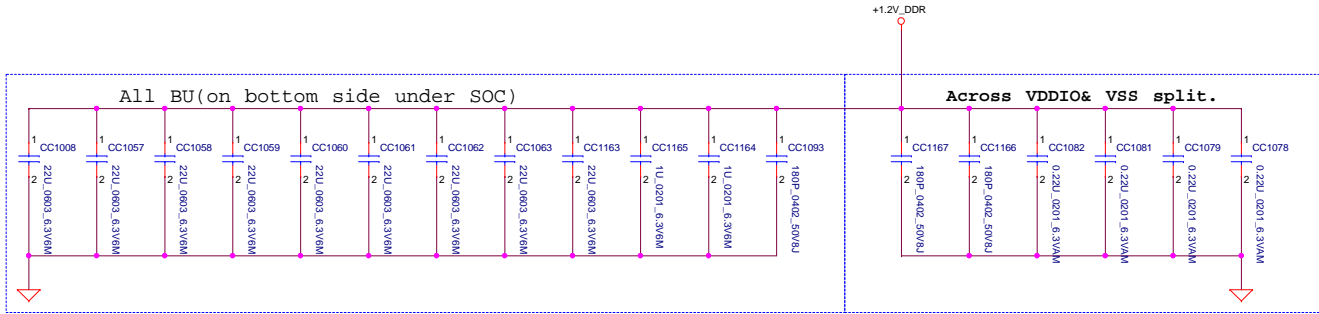
Function	EGPIO70
ULTRA BAY	1
NO ULTRA BAY	0

Function	AGPIO90
S_BATT	1
NONS_BATT	0

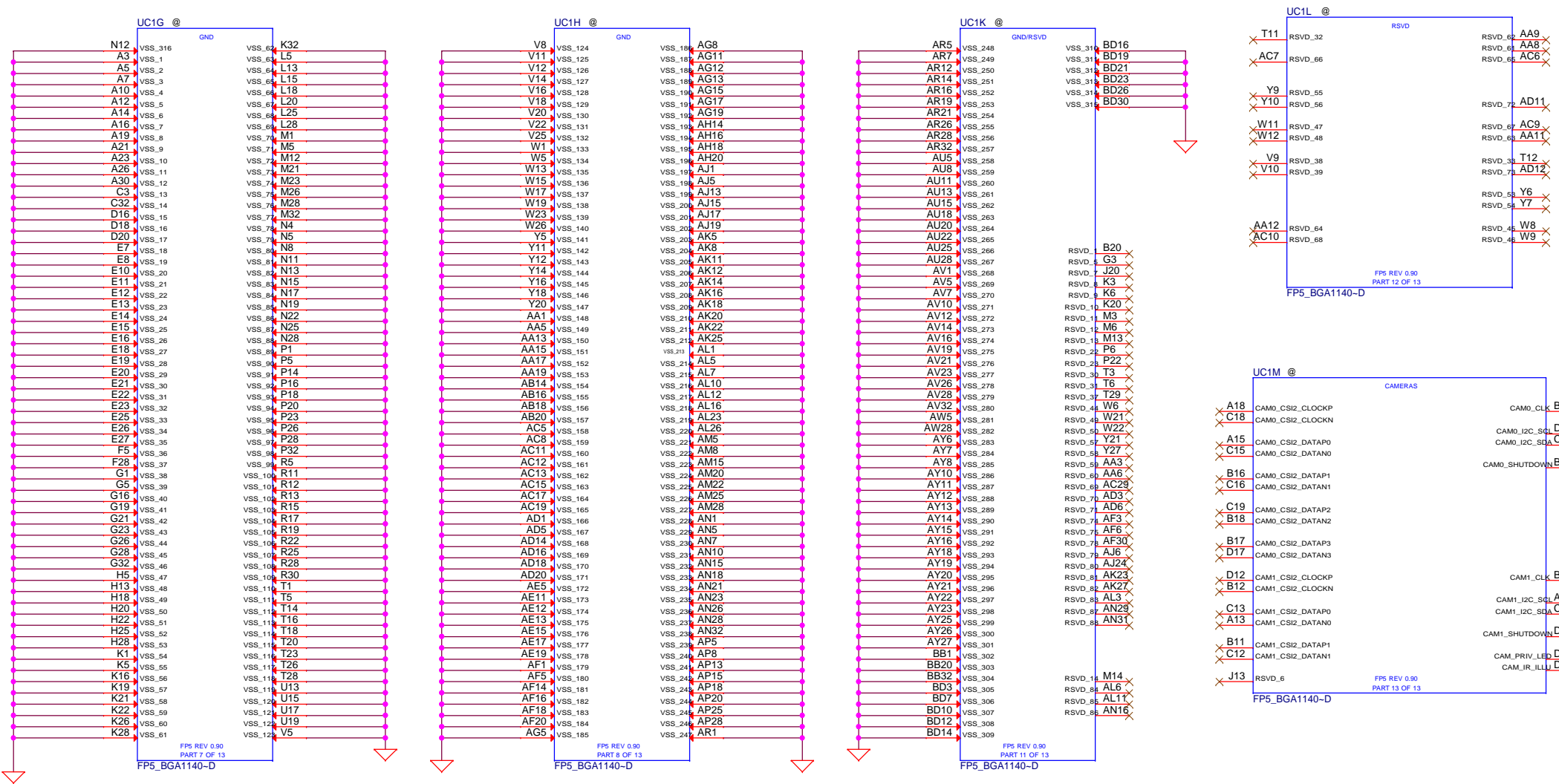




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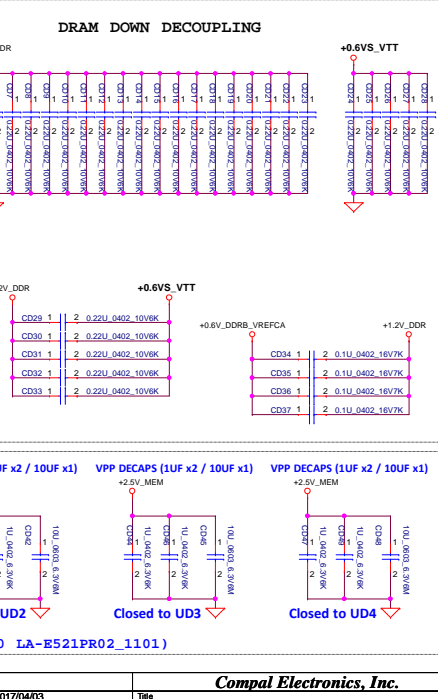
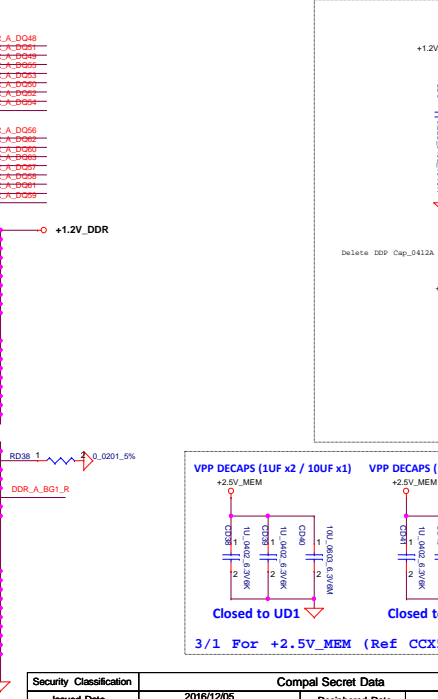
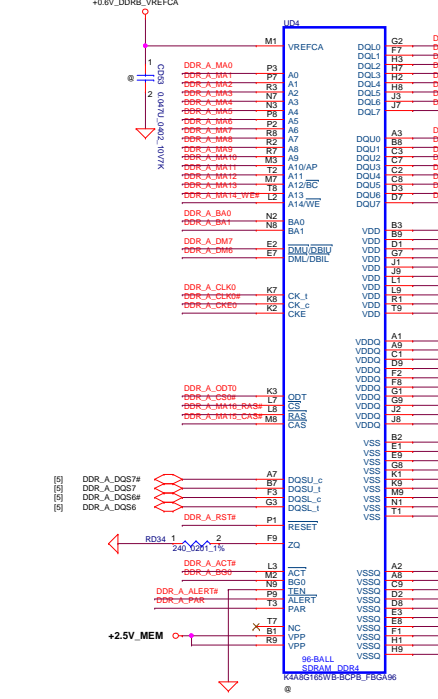
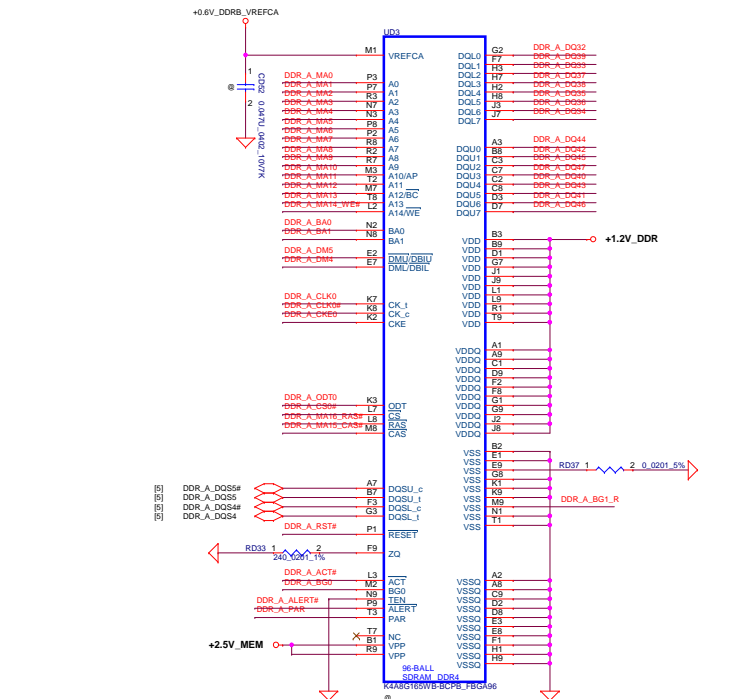
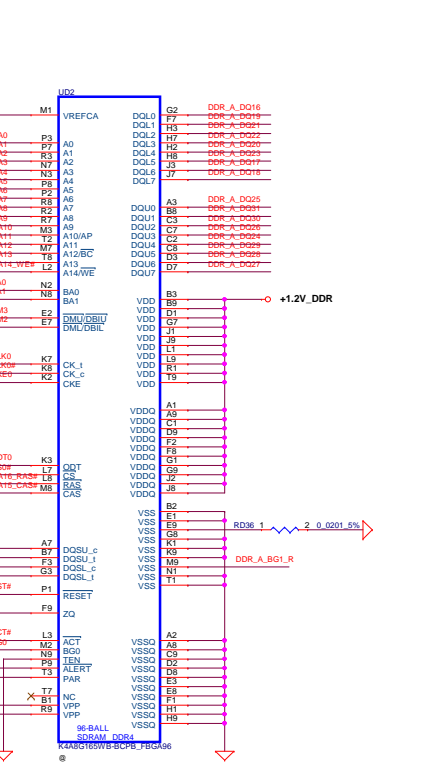
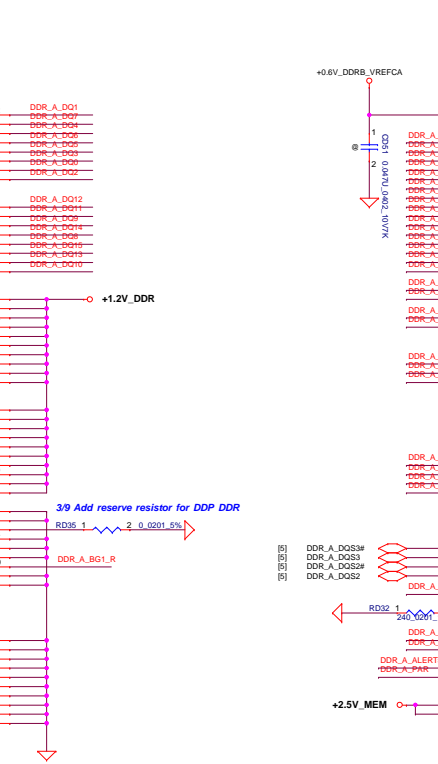
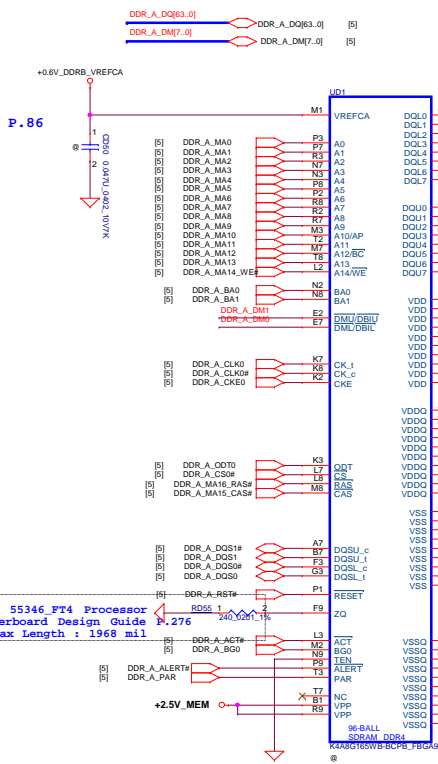
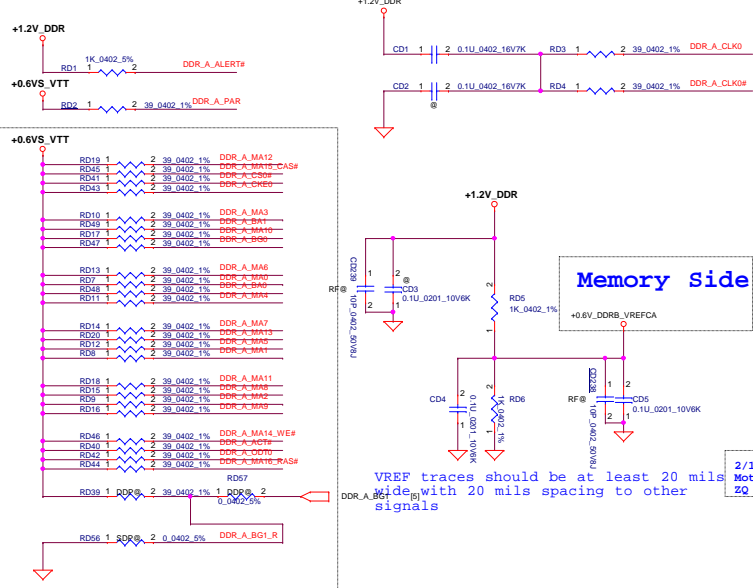
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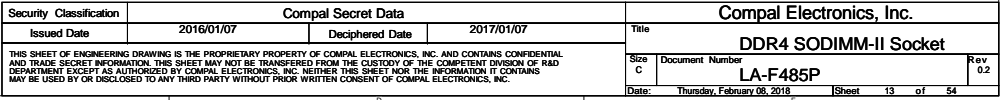
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Memory Down

5/10A 55597\_FP5 Processor Motherboard Design Guide P.86



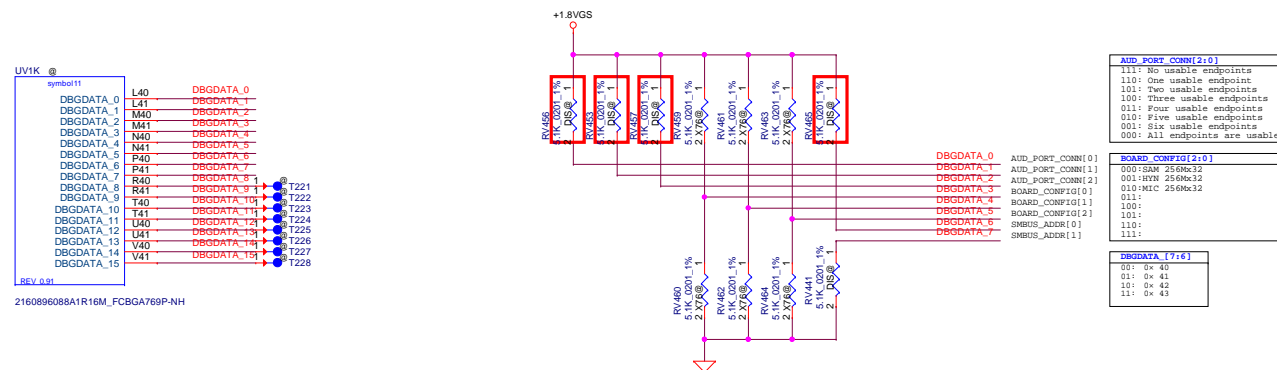
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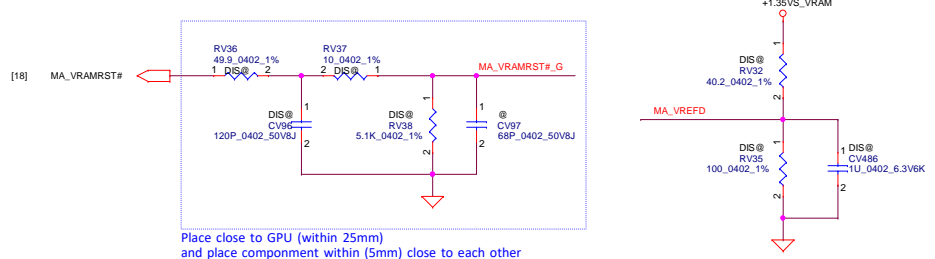
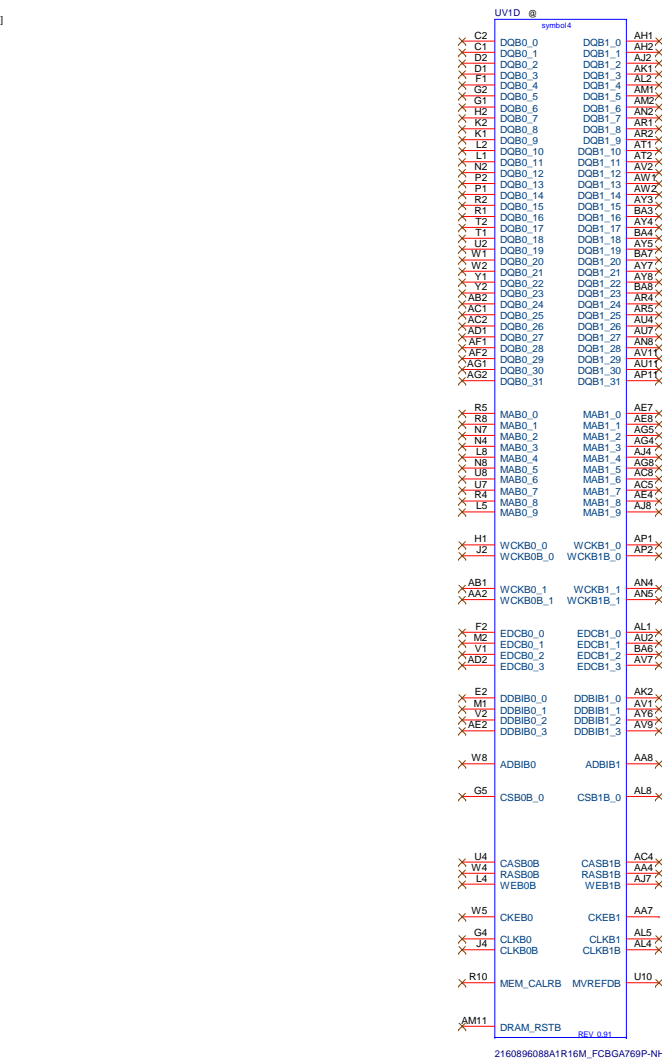
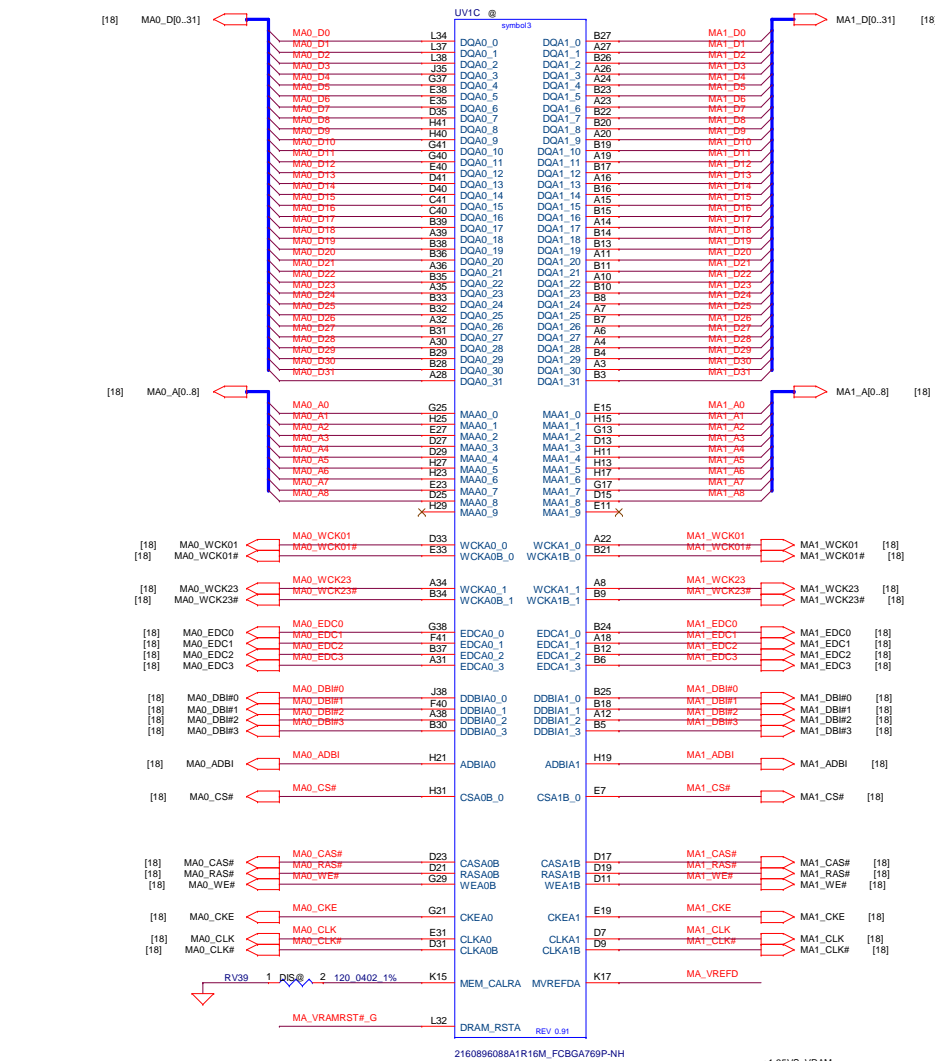




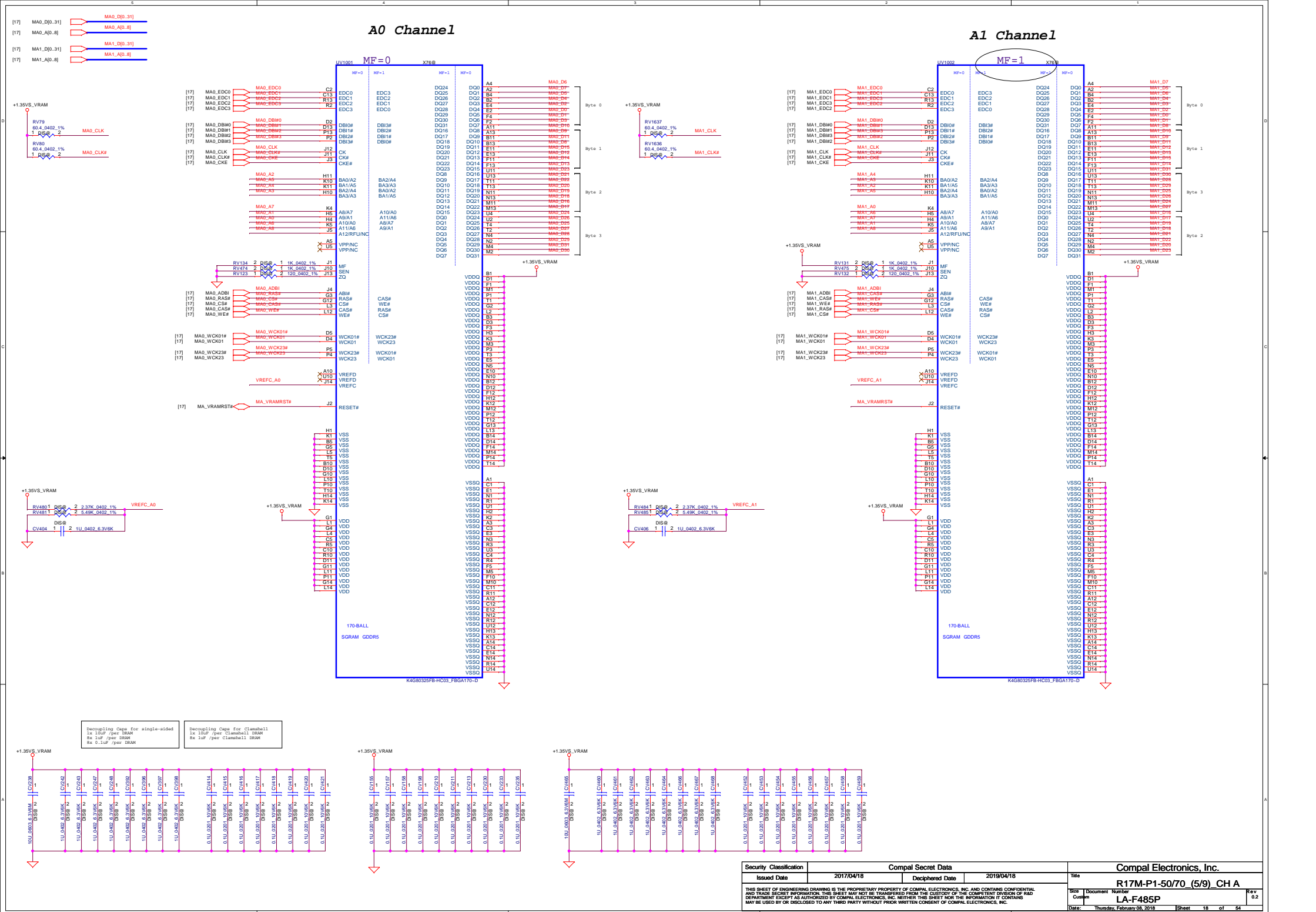


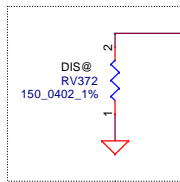
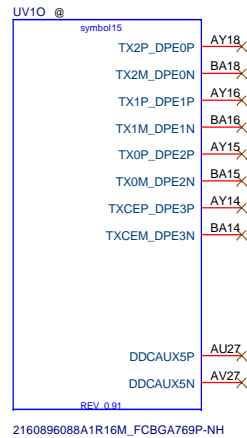
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ID	[2:0]						
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1	001	Samsung-GDDR5	256M x32 2PCS, 1 BANK		2GB	44GB80325F8-HC8R	2 pcs
2	010	Hynix-GDDR5	256M x32 2PCS, 1 BANK		2GB	H5GC8H24M8R-0C	2 pcs
3	011	Micron-GDDR5	256M x32 2PCS, 1 BANK		2GB	MTS1J256M32HF	2 pcs
4	100						
5	101						
6	110						
7	111						



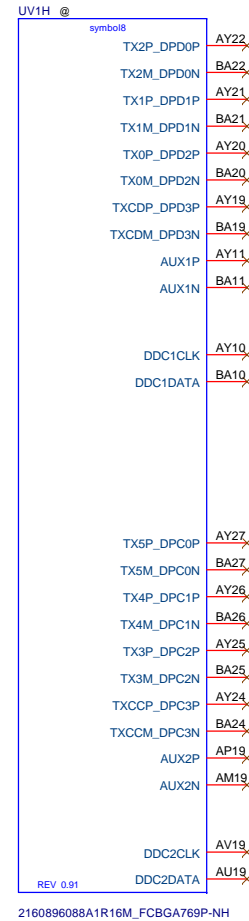
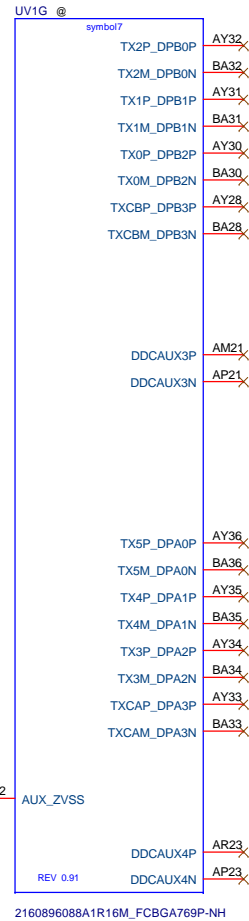


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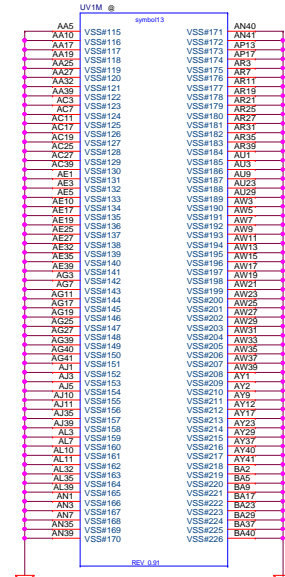
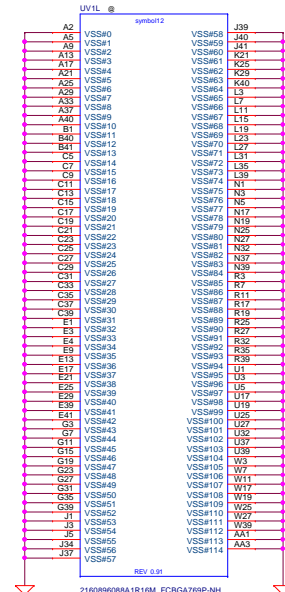
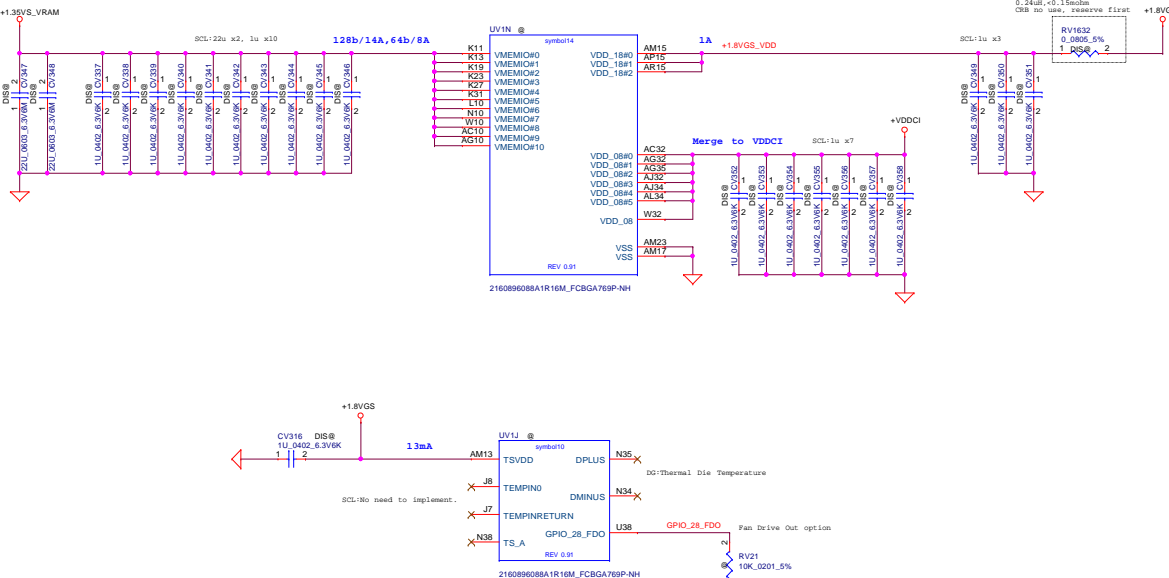




Data Book: need  
config even if not  
use display function



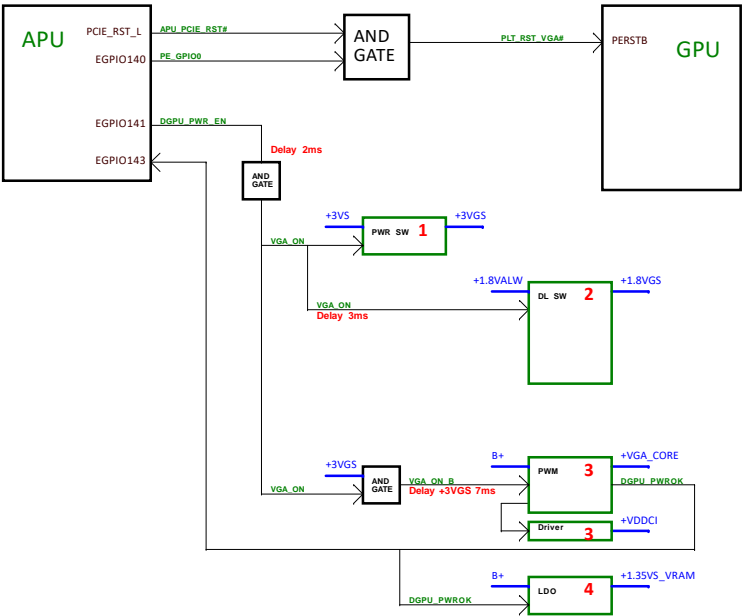
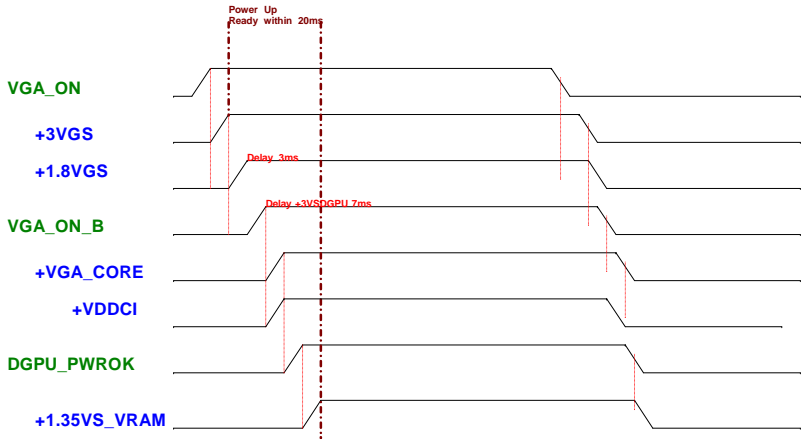
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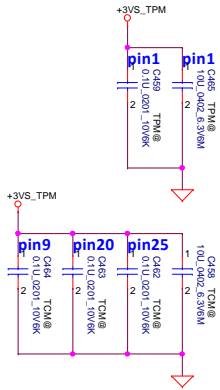


5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

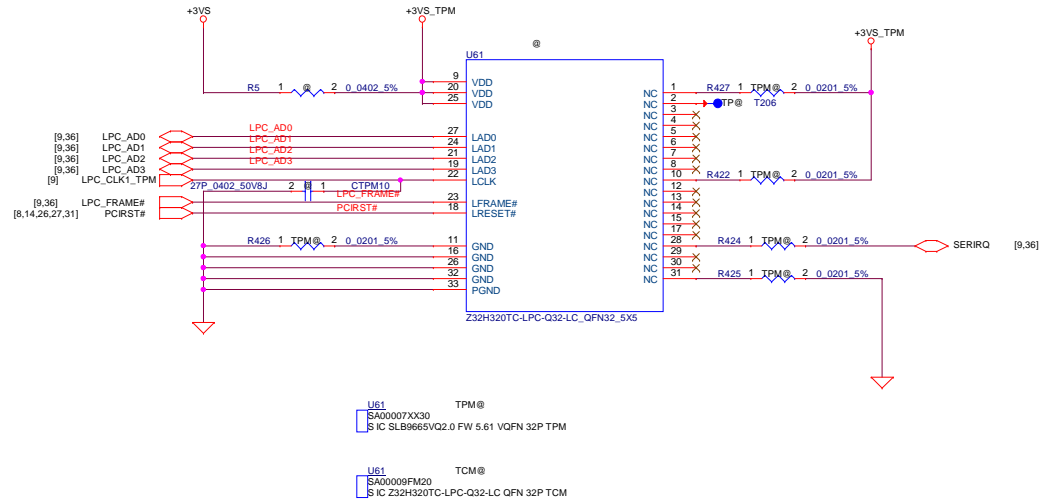
- All the GPU supplies, except for VDD\_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD\_08, and VMEMIO start to ramp up.



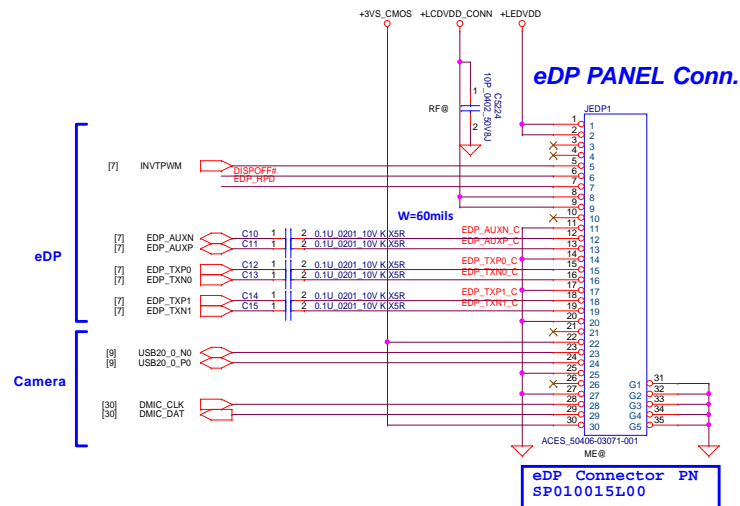
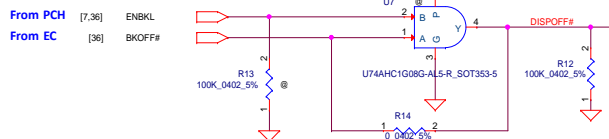
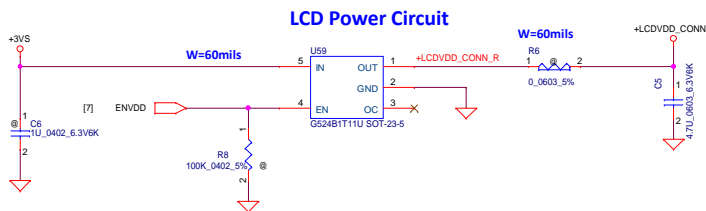
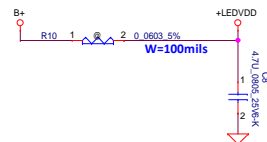
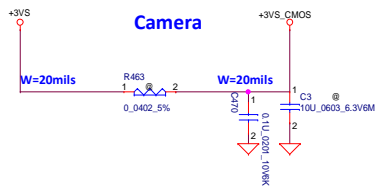


R5  
SD028000080 TPM@  
S RES 1/16W 0 +5% 0402

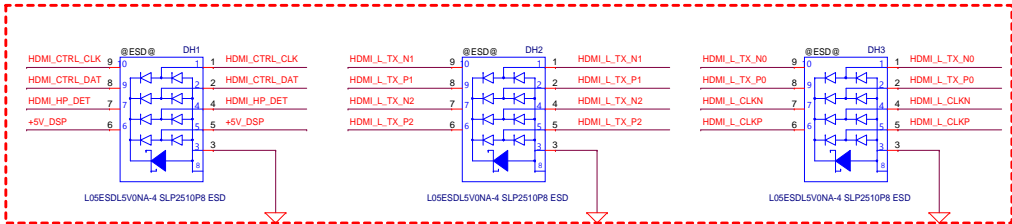
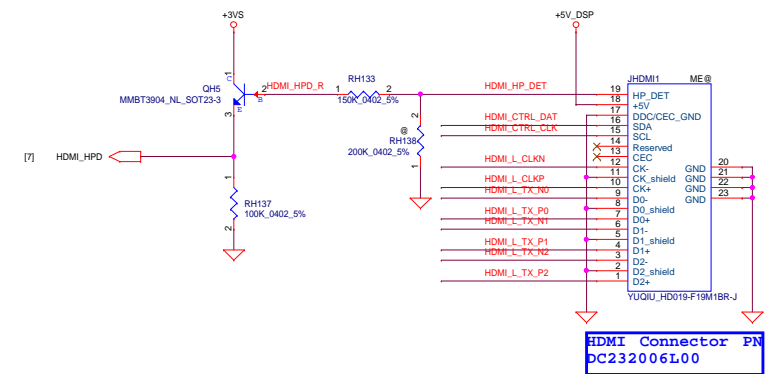
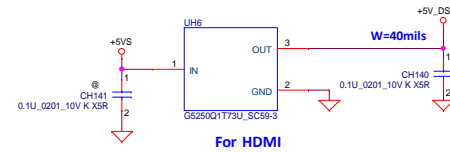
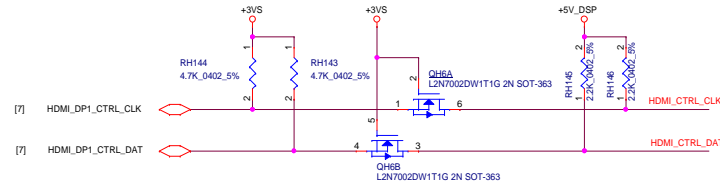
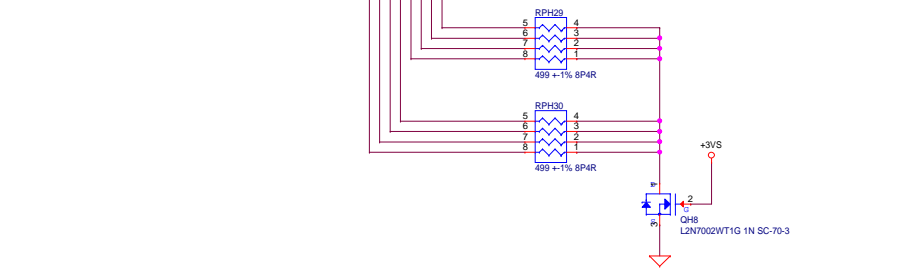
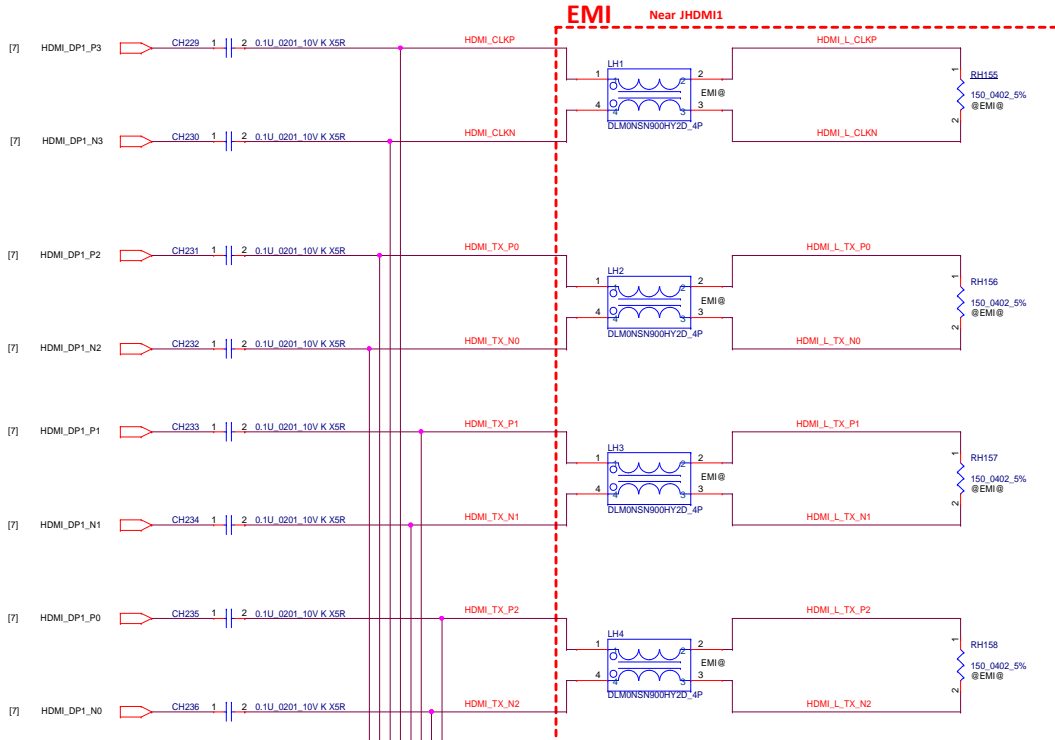
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S RES 1/16W 0 +5% 0402



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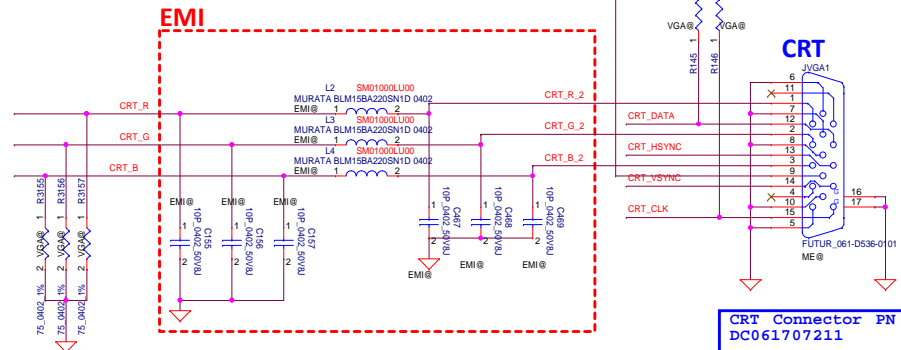
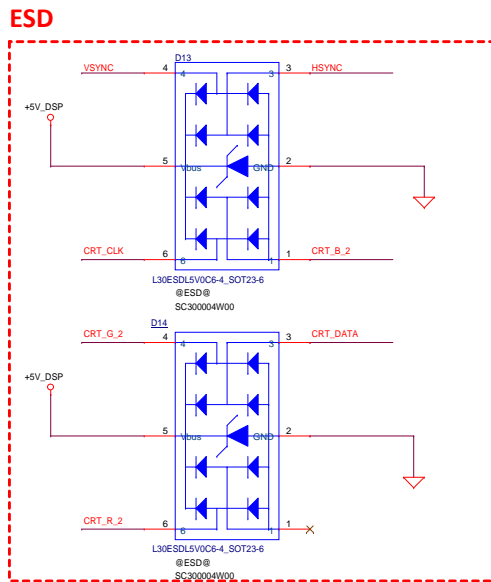
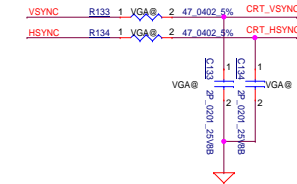
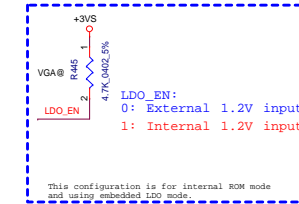
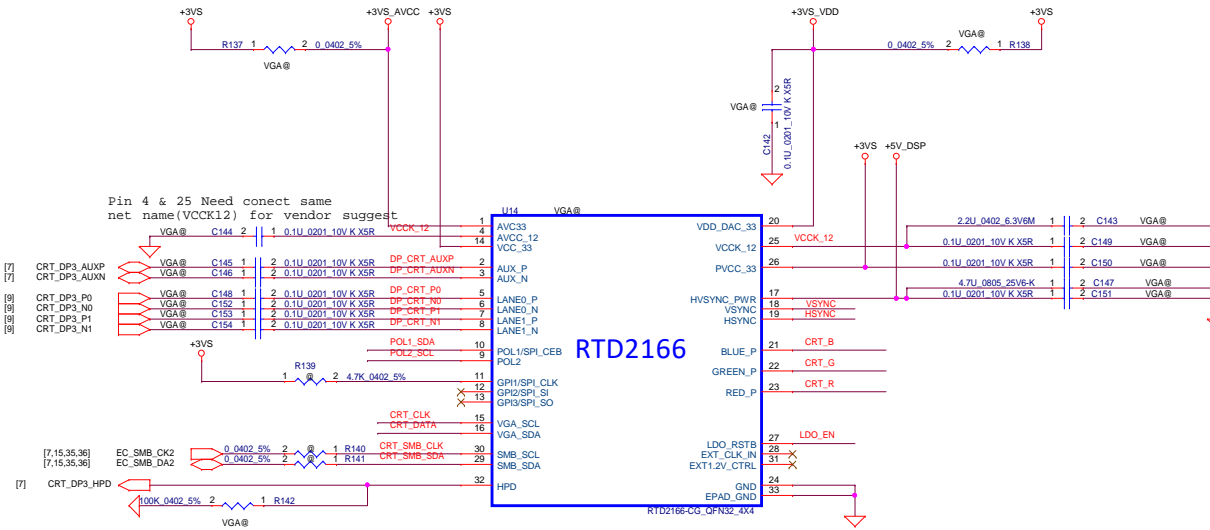
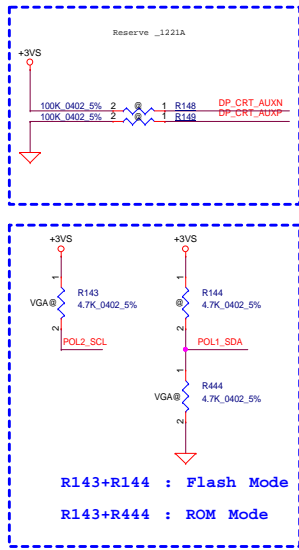


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Issued Date	2016/12/05	Deciphered Date	2017/04/03	eDP/CAMERA	
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				Date: Thursday, February 08, 2018	Sheet 23 of 54

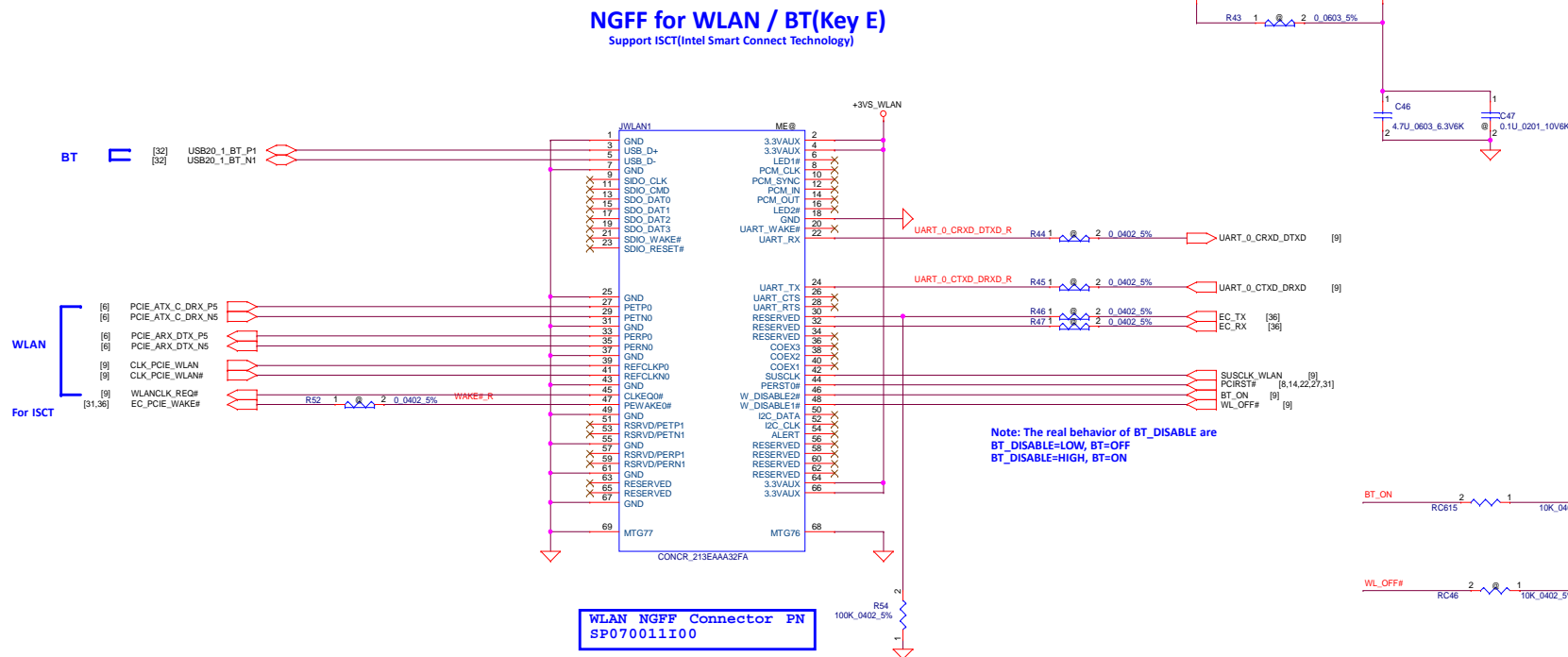


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Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title	HDMI
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				Date: Thursday, February 08, 2018	Sheet 24 of 54

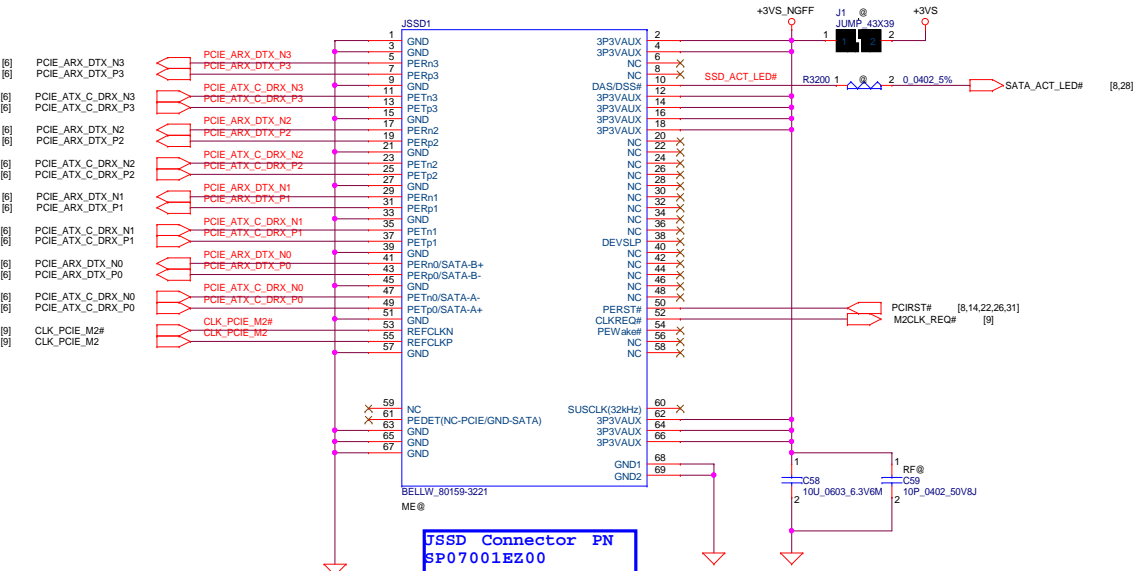




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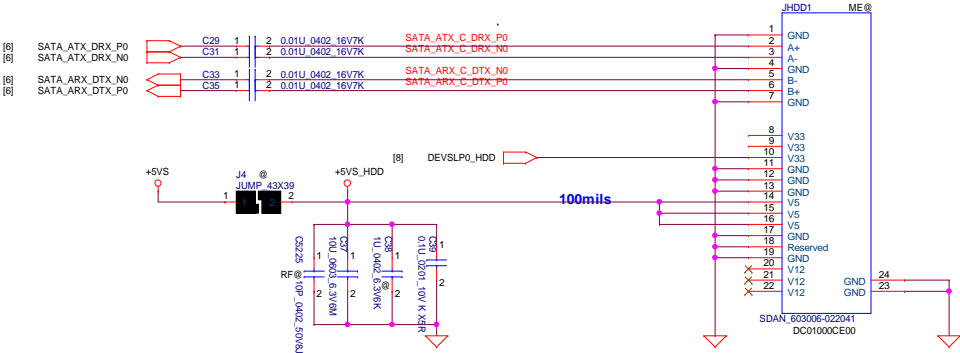
M.2 mSATA Conn



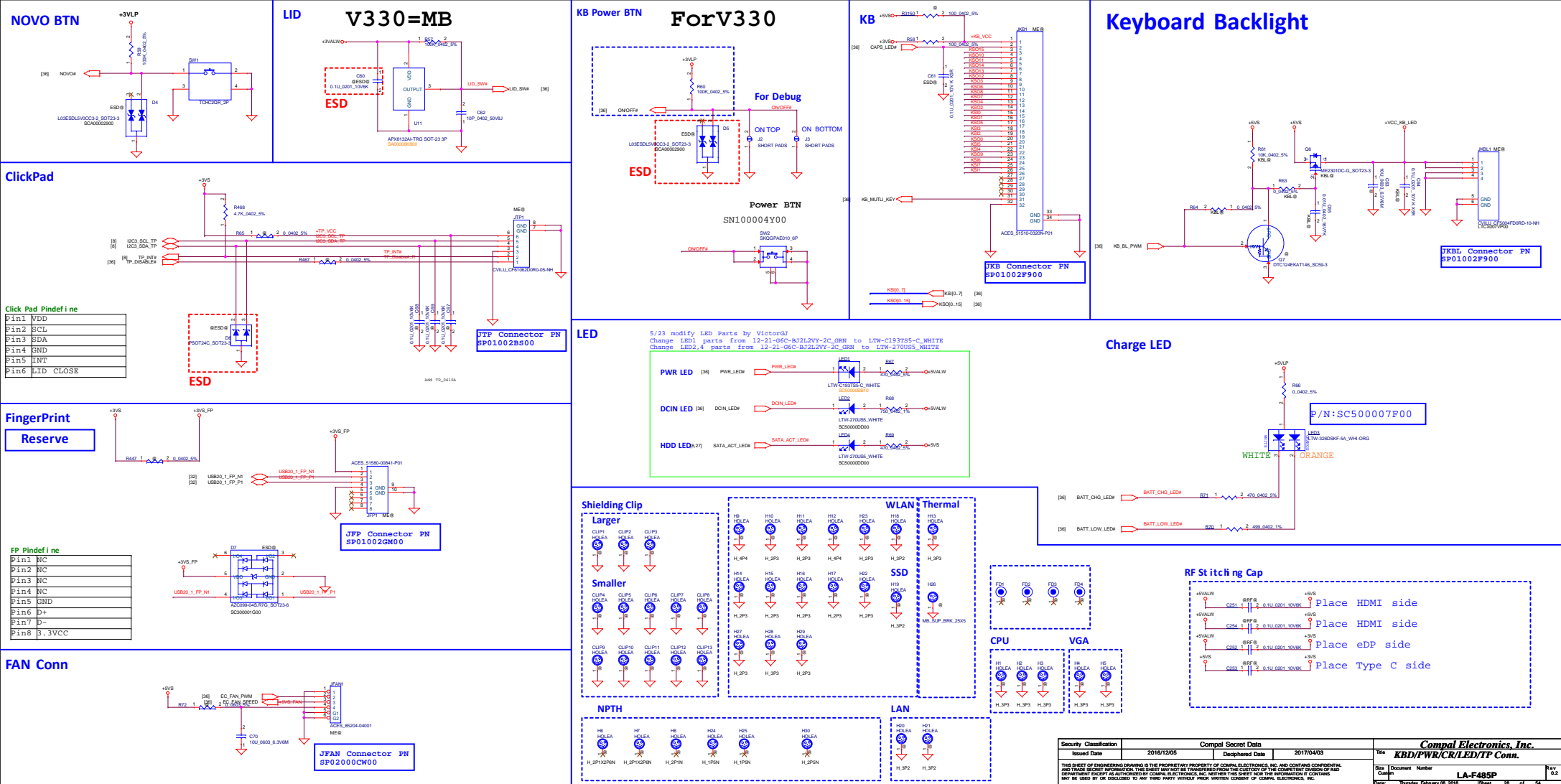
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HDD

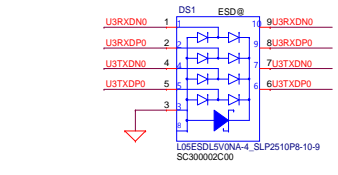
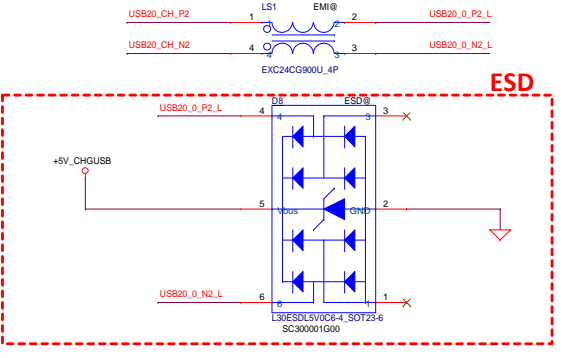
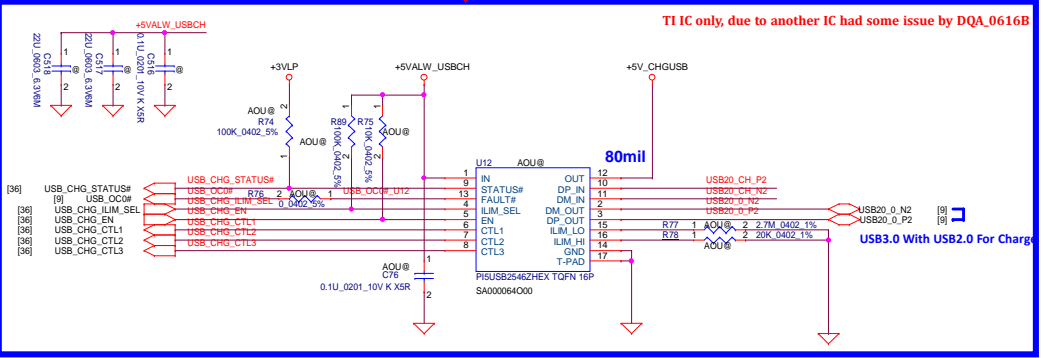
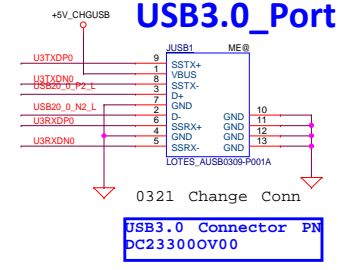
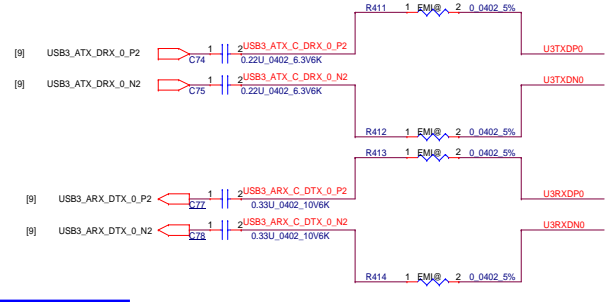
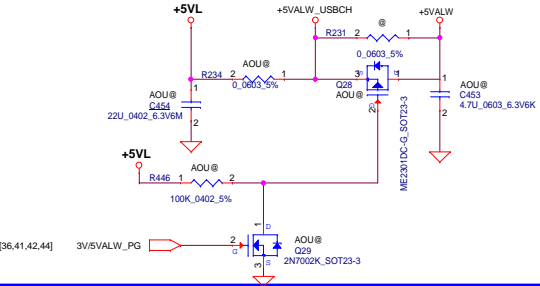
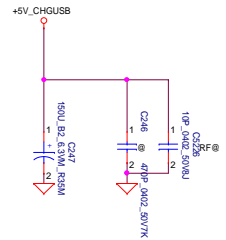
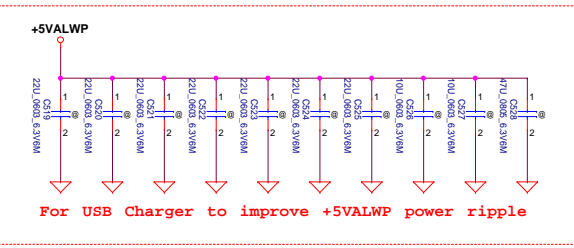
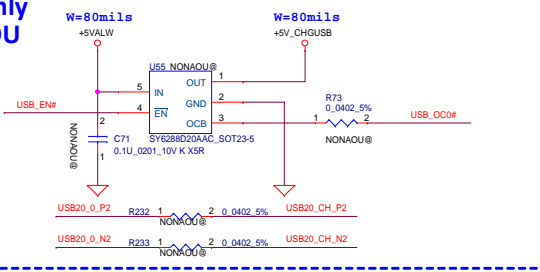
SATA HDD Conn.



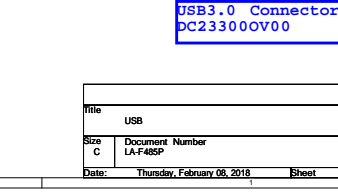
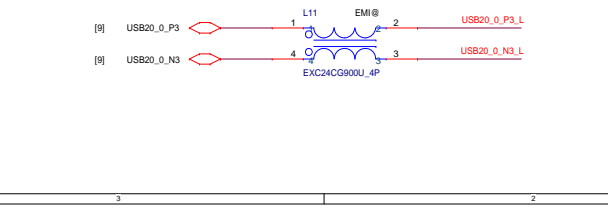
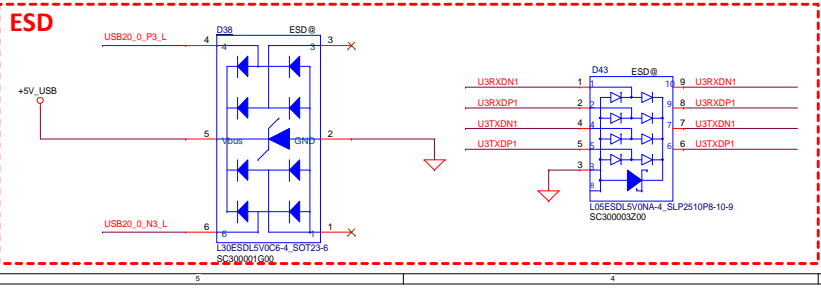
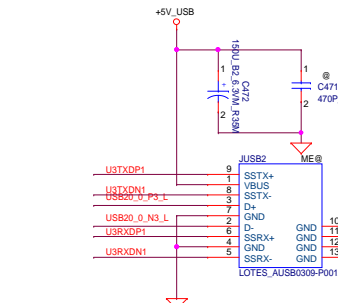
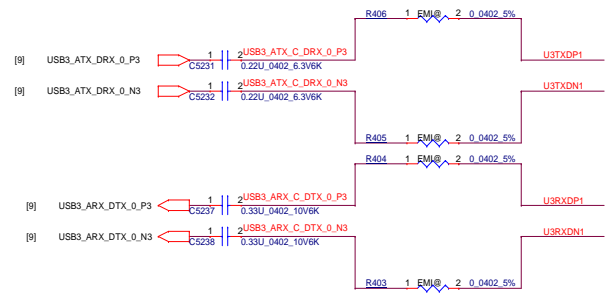
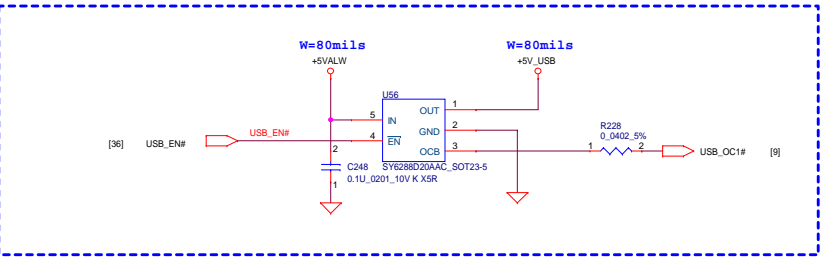
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title	M.2 SSD/HDD
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USB 3.0 V330 only NONAOU

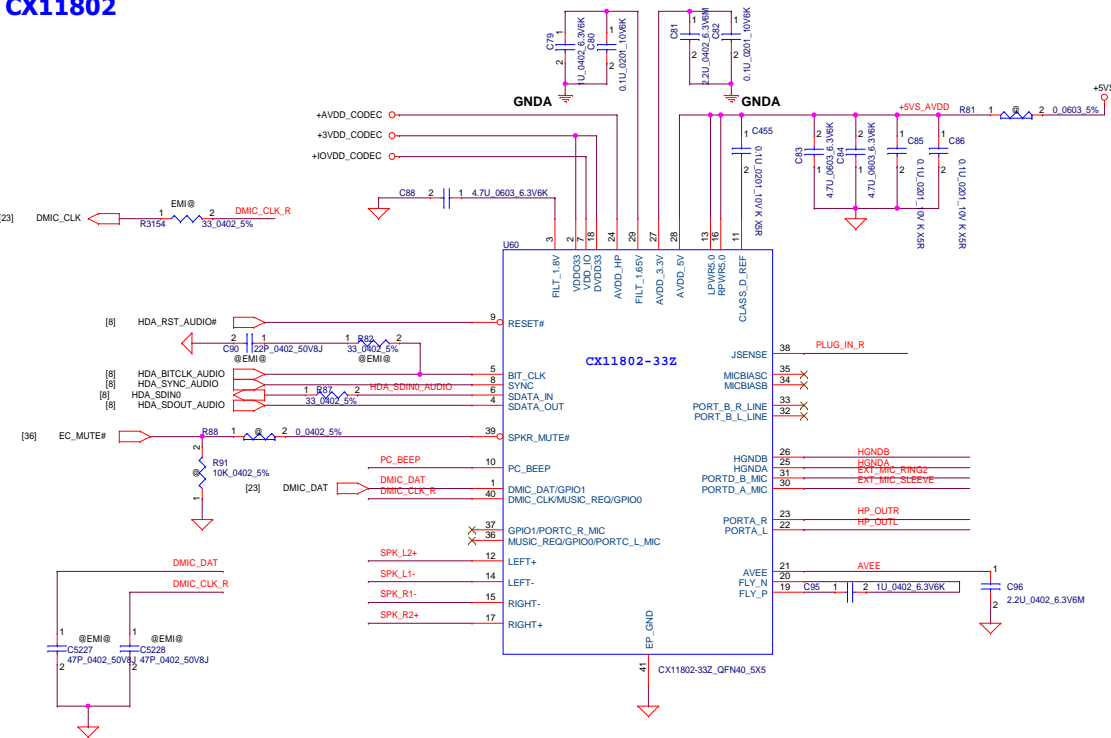


USB 3.0 Right side

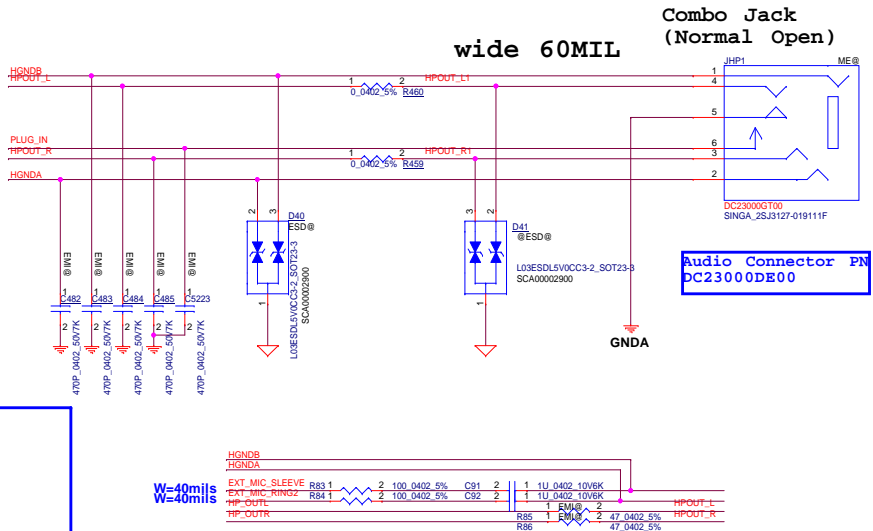


Title			USB
Size	Document Number	Rev	
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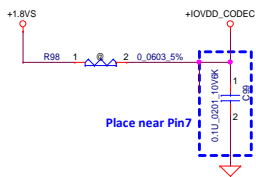
# CX11802



## Combo Jack

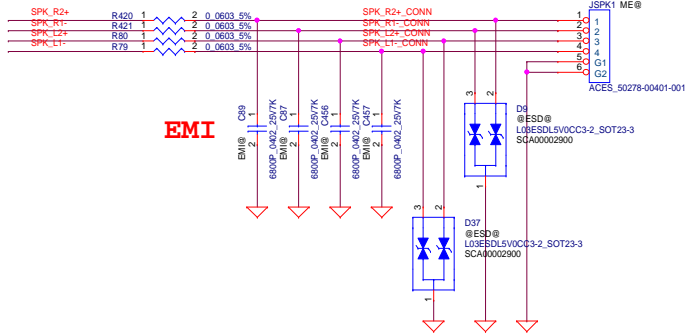


**+1.8VS → +1 OVDD\_CODEC**

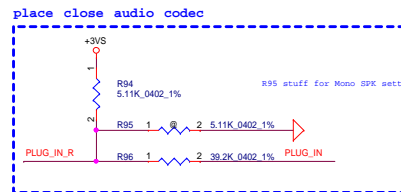


**Speaker**

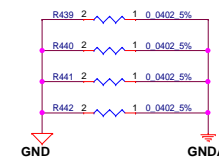
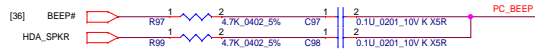
wide 40MIL



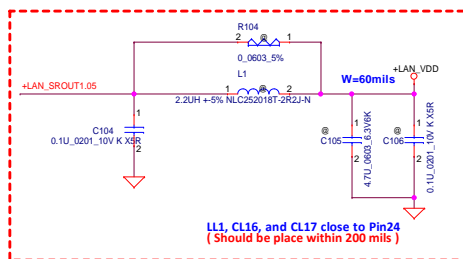
Speaker Connector PN  
SP02000RR00



## PC Beep

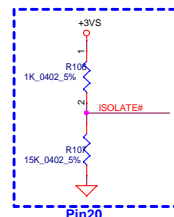
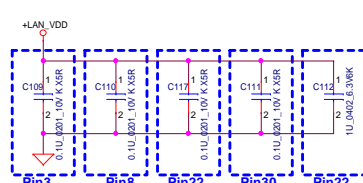
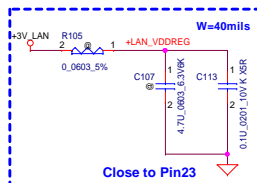
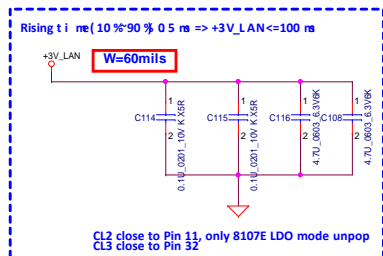


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				Size	Document Number	Rev
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Date:		Thursday, February 08, 2018		Sheet	30	of 54

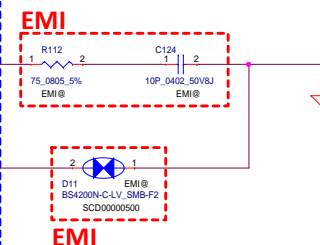
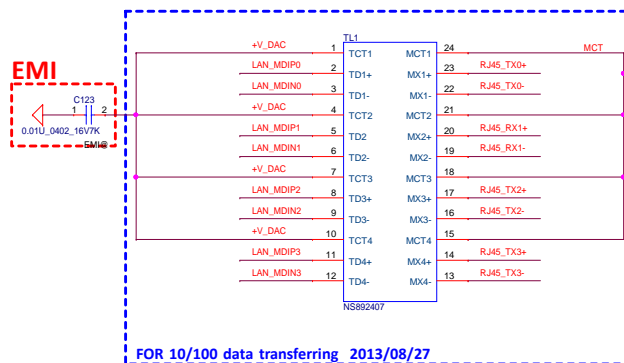
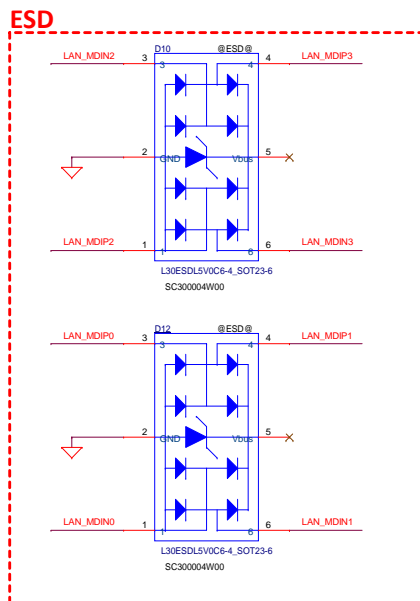
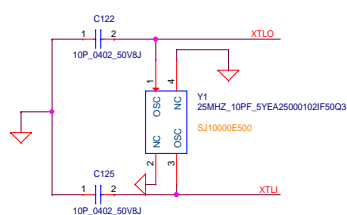
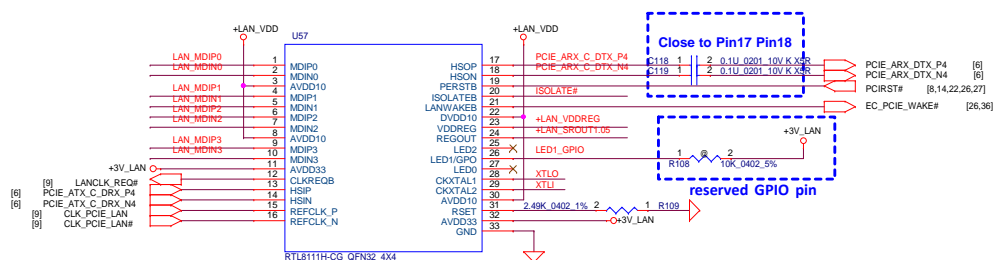
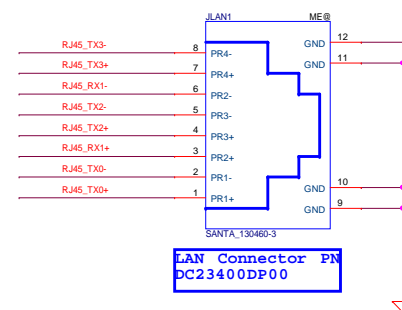


	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

Please refer to the table above when using different 1.0V supply source.

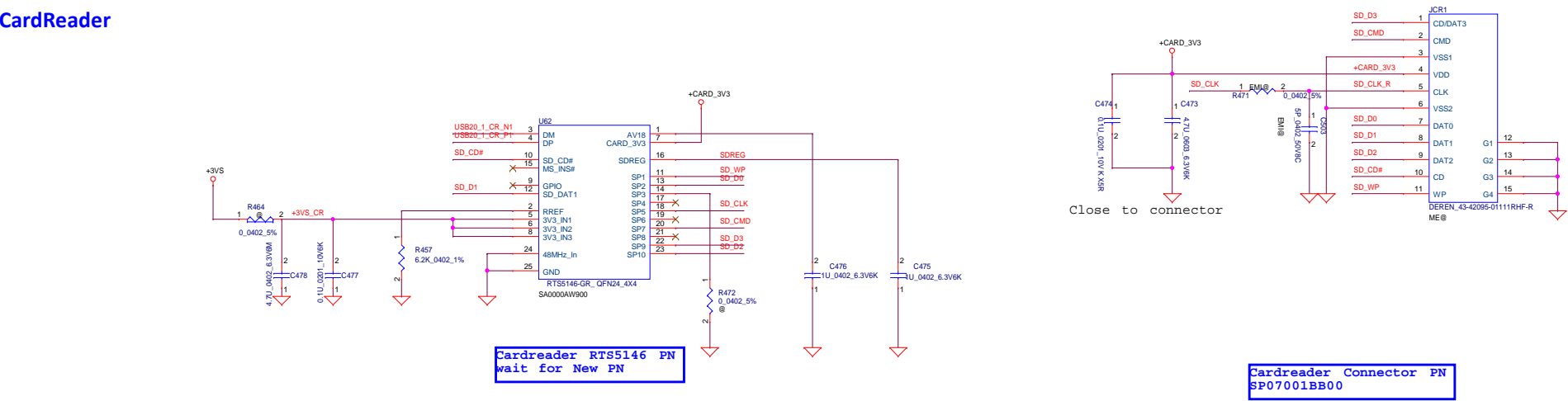


## RJ-45 CONN.

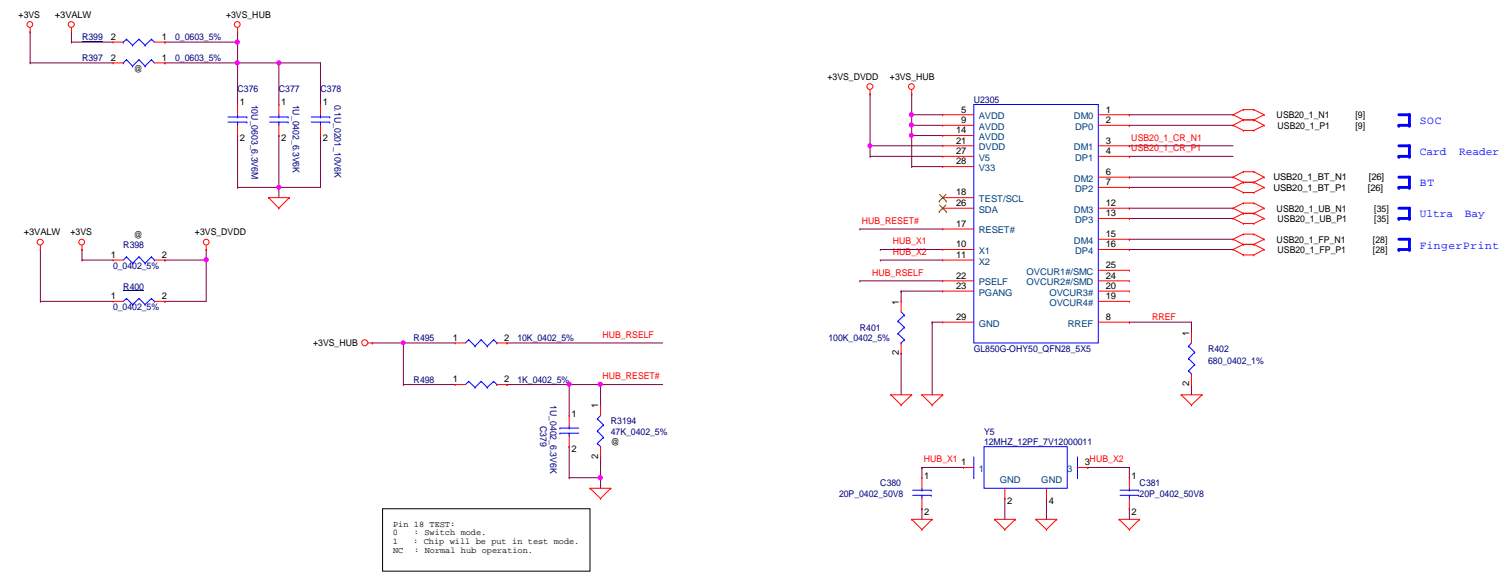


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				Size	Document Number	Rev
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CardReader

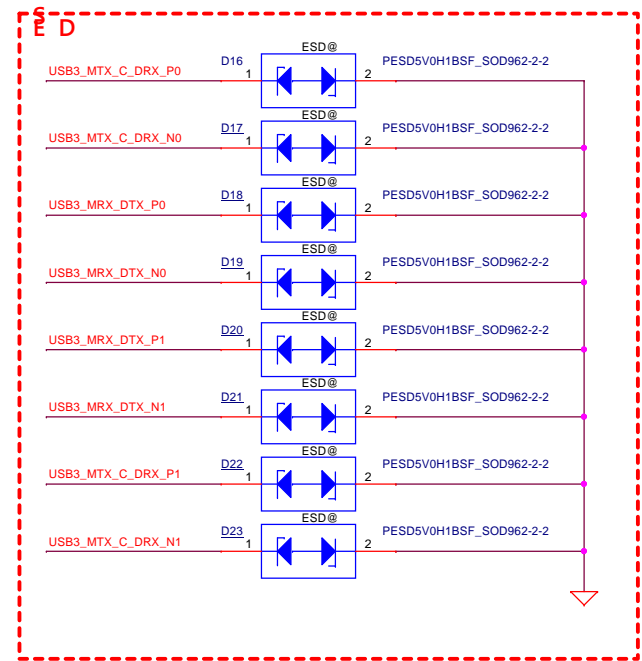
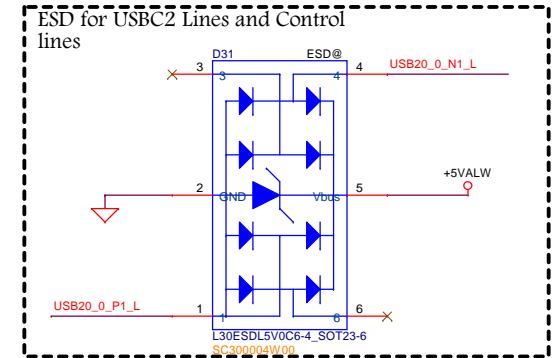
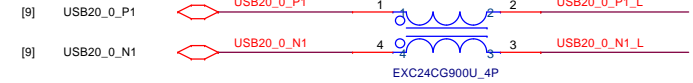
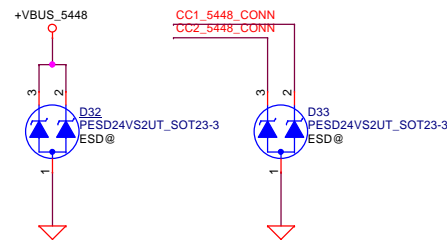
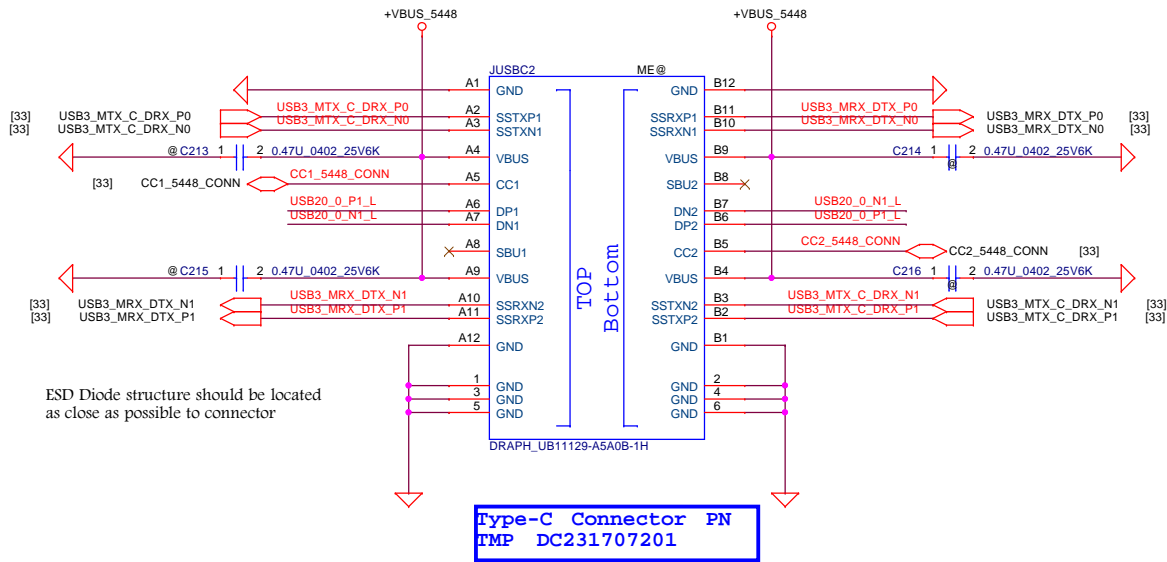


USB20 HUB



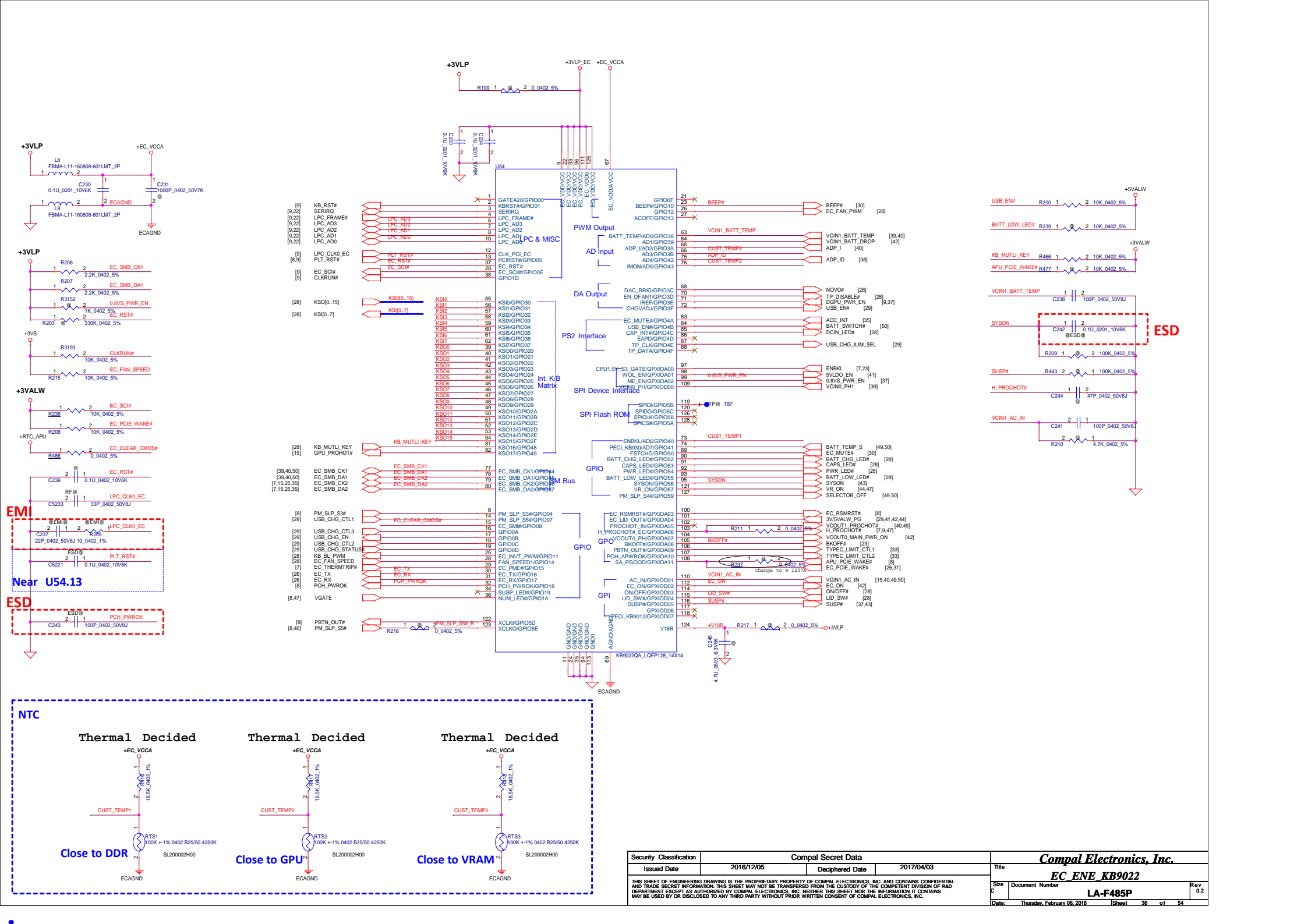






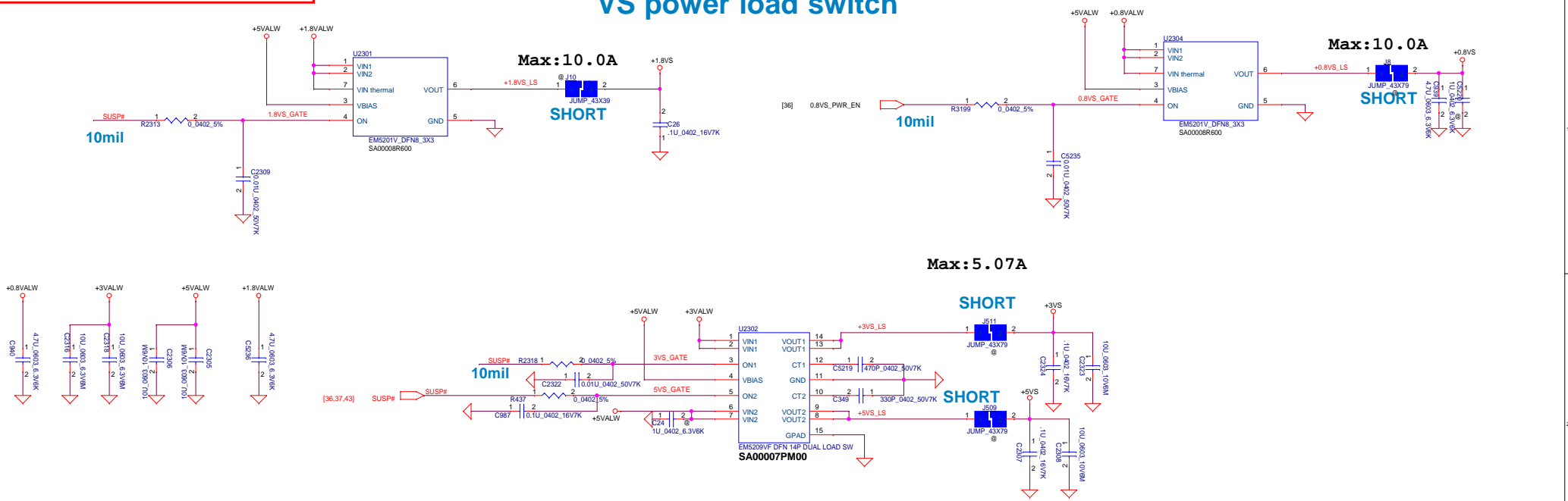
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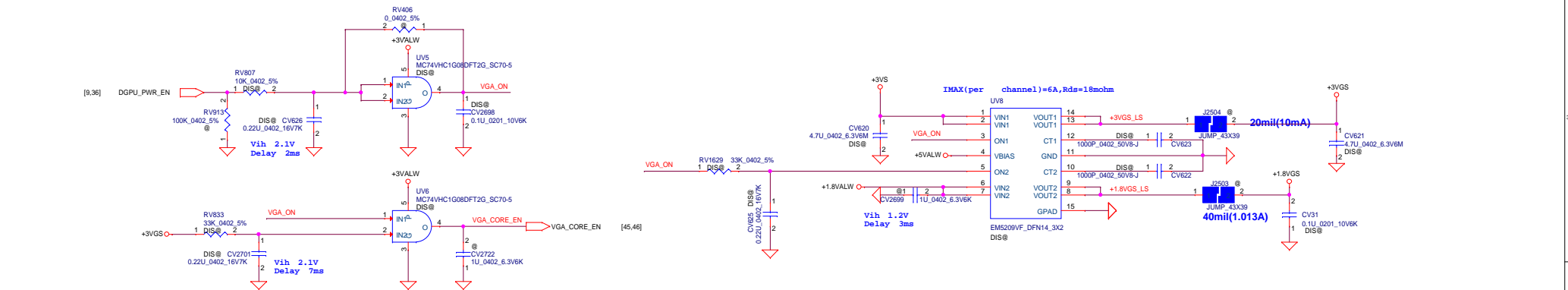


Main Func = DC Interface

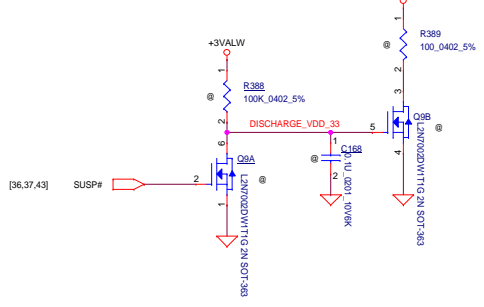
VS power load switch



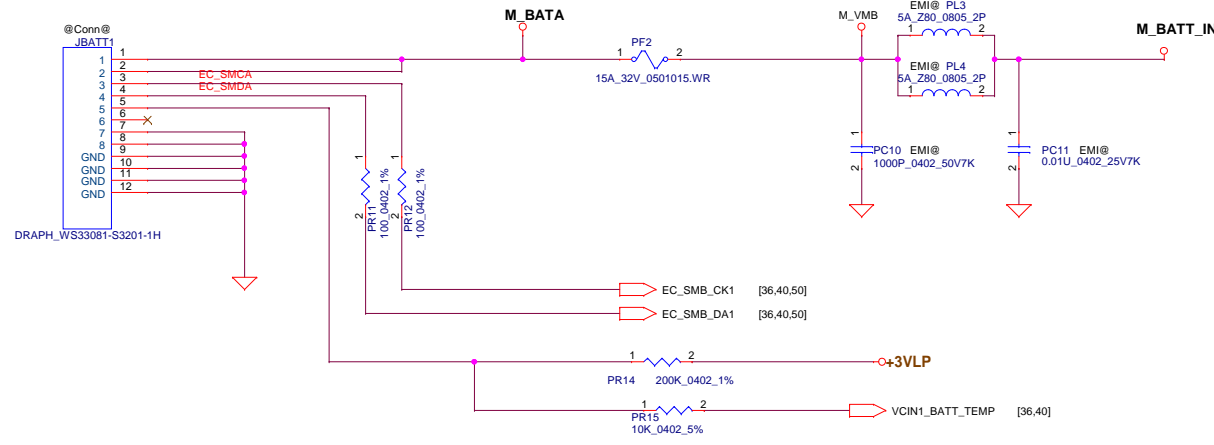
dGPU power load switch



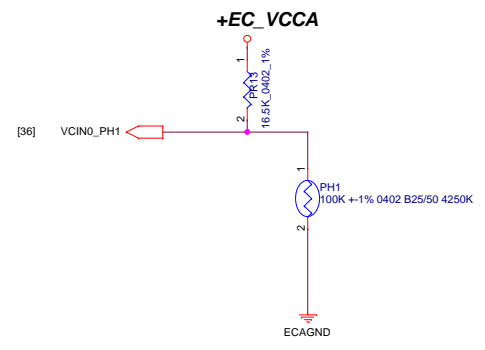
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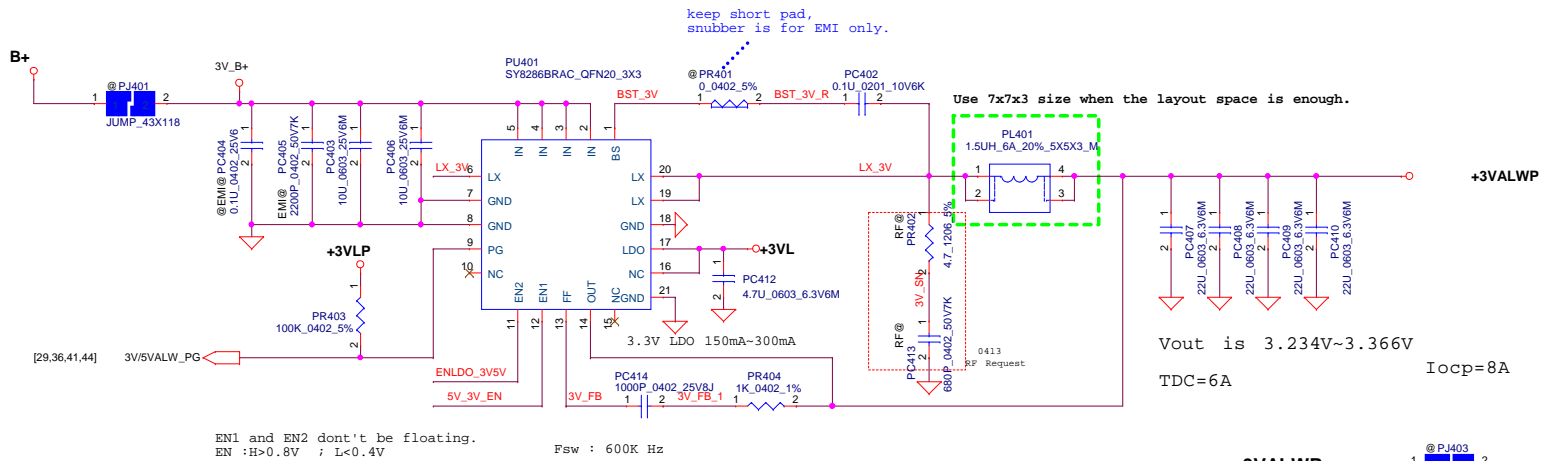
PH201 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C





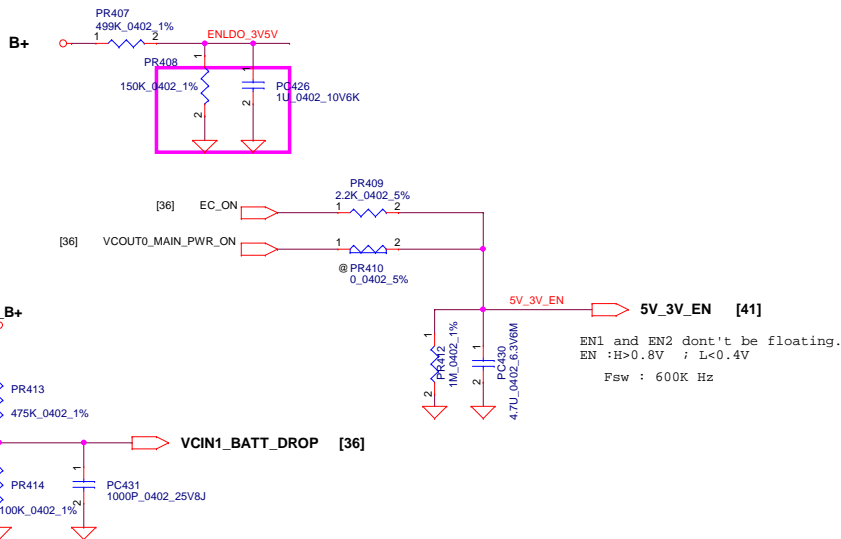




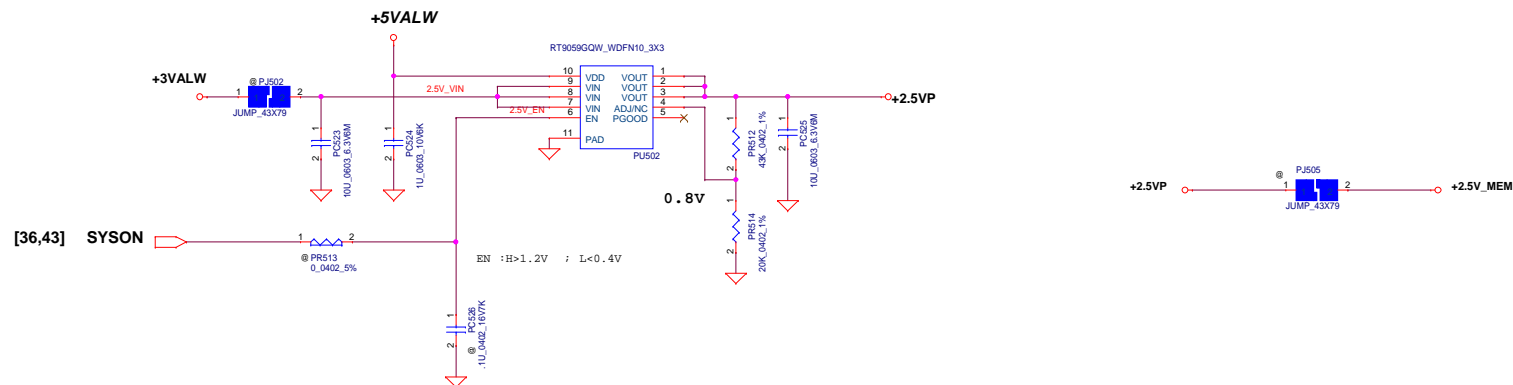
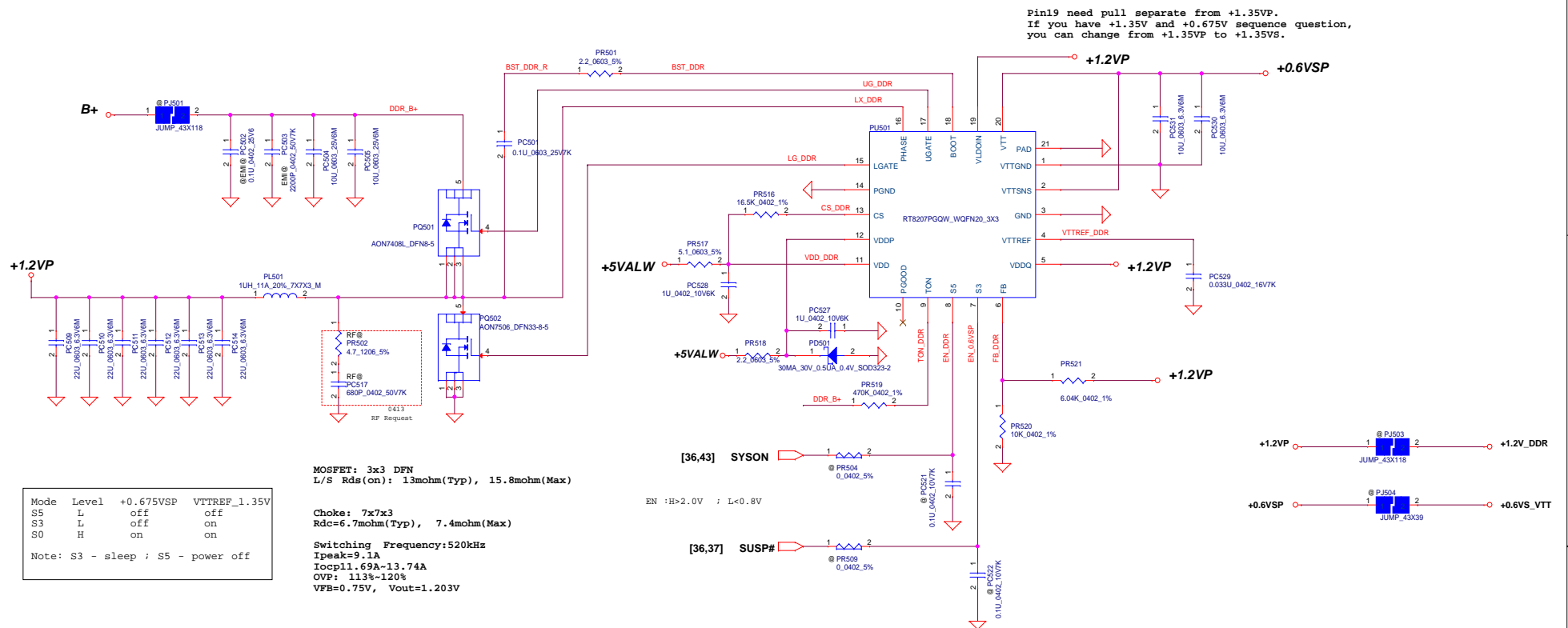


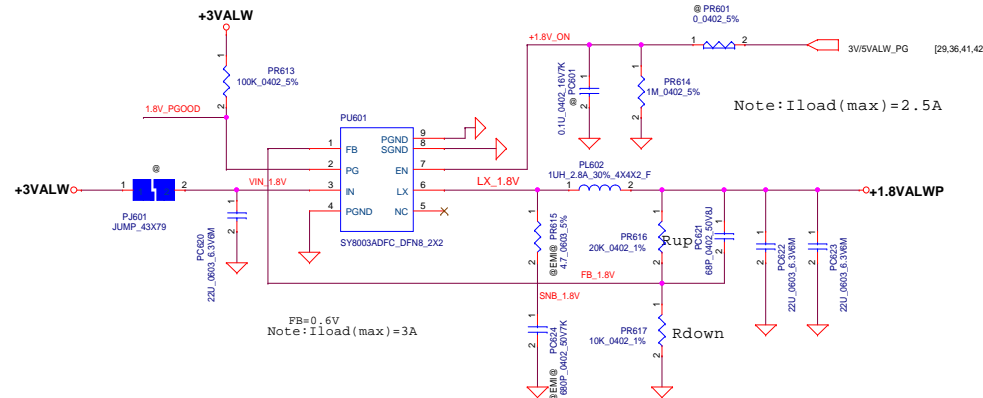
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JUMP\_43X118

+3VL @PJ404  
JUMP\_43X39

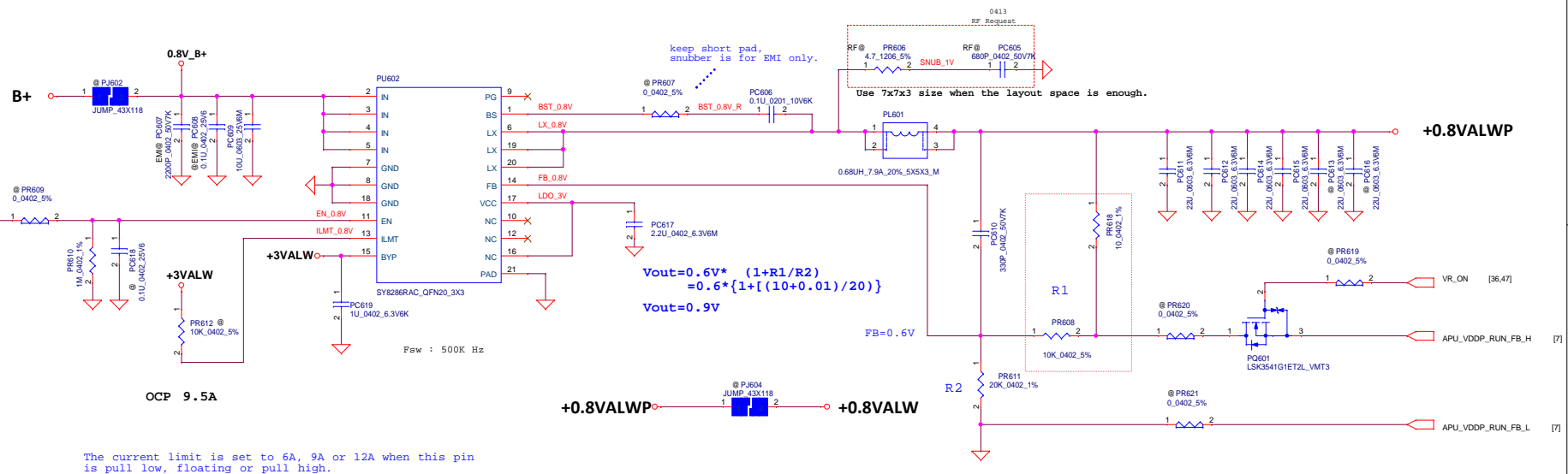
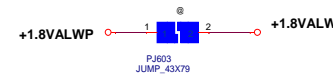


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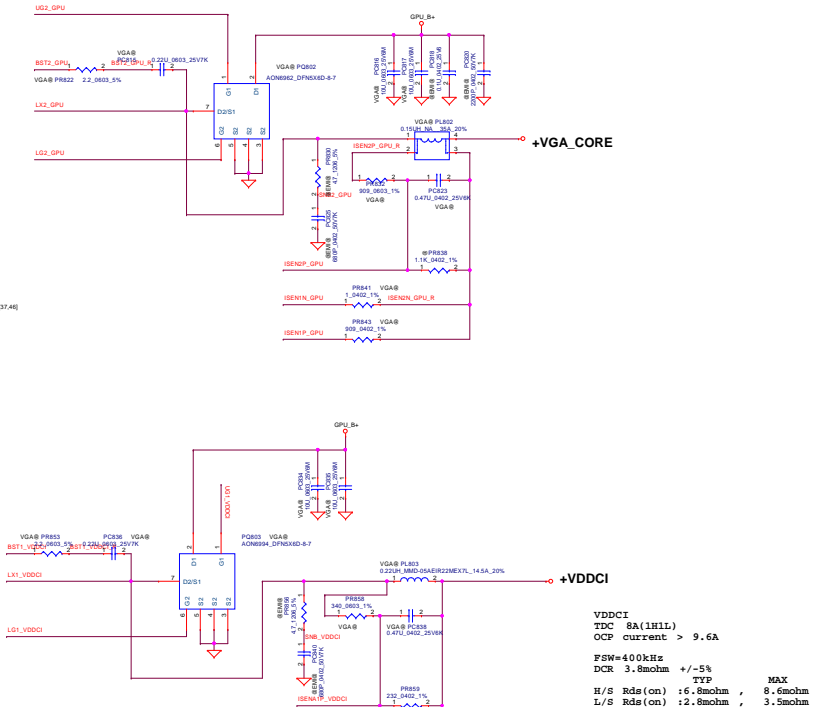
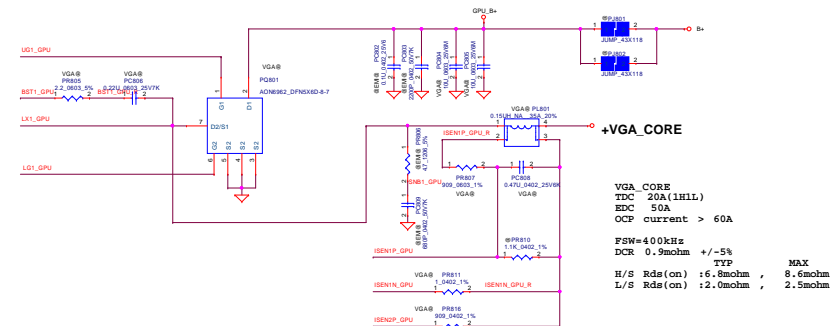
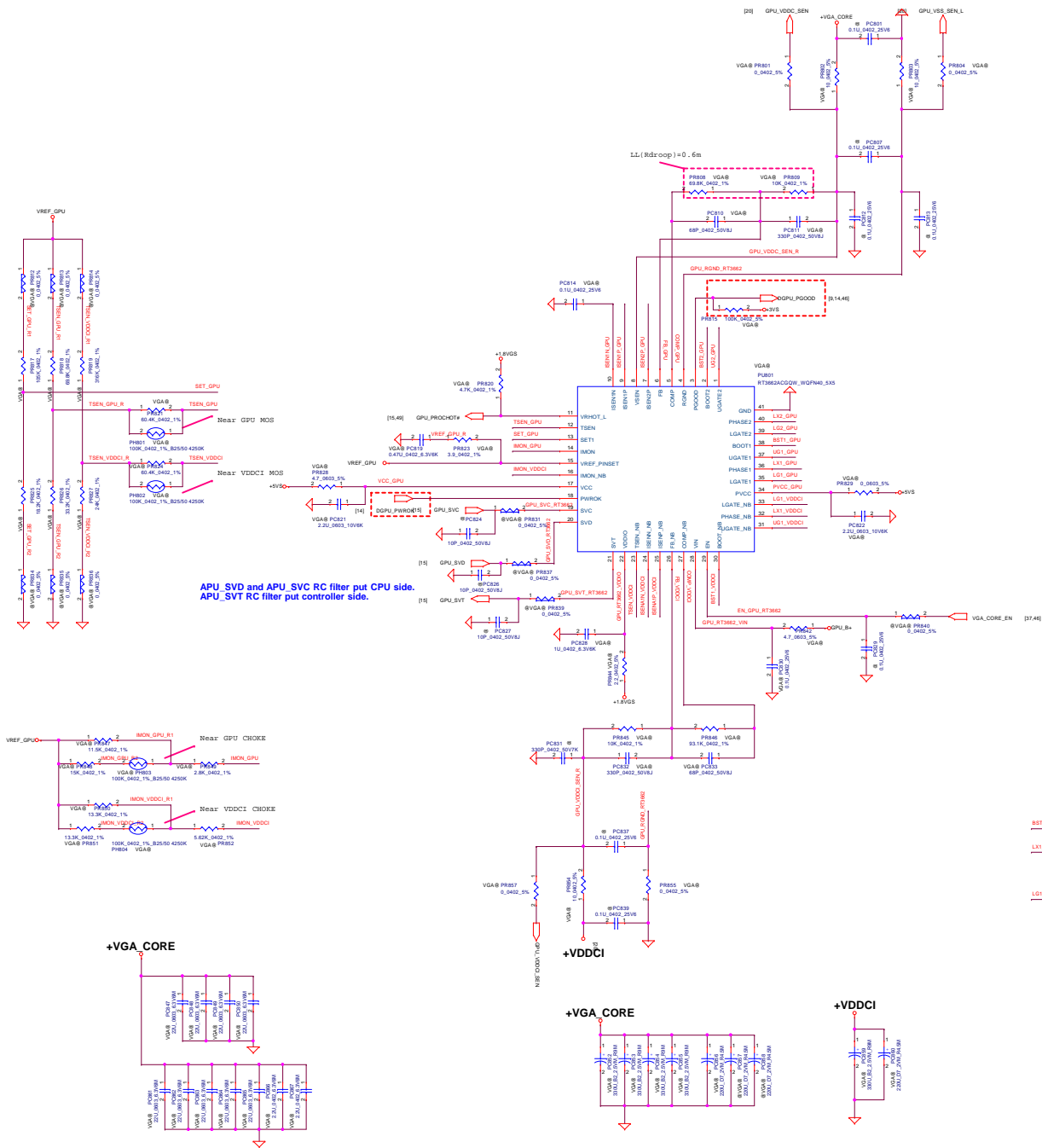




Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage



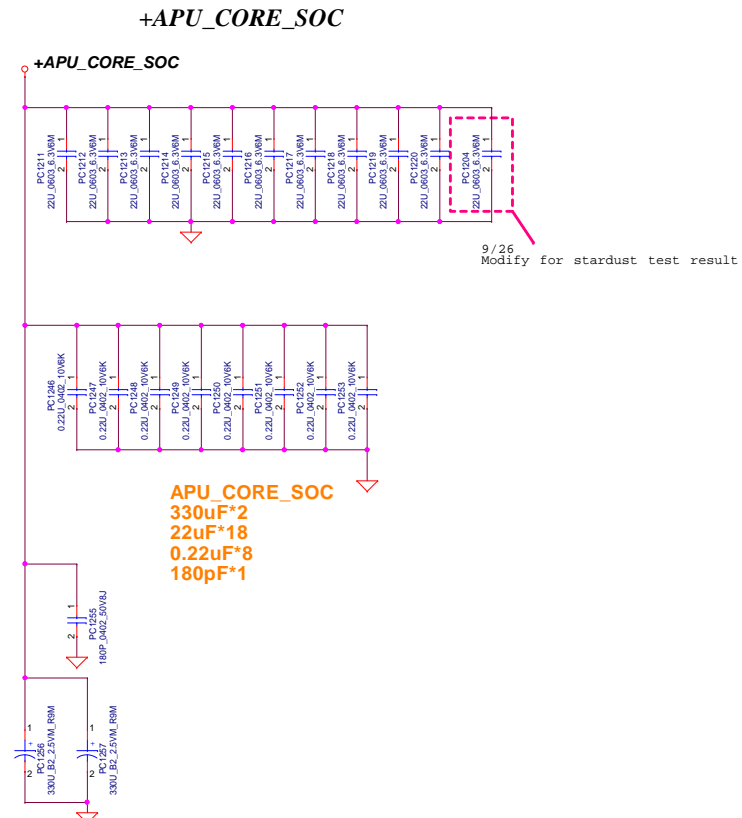
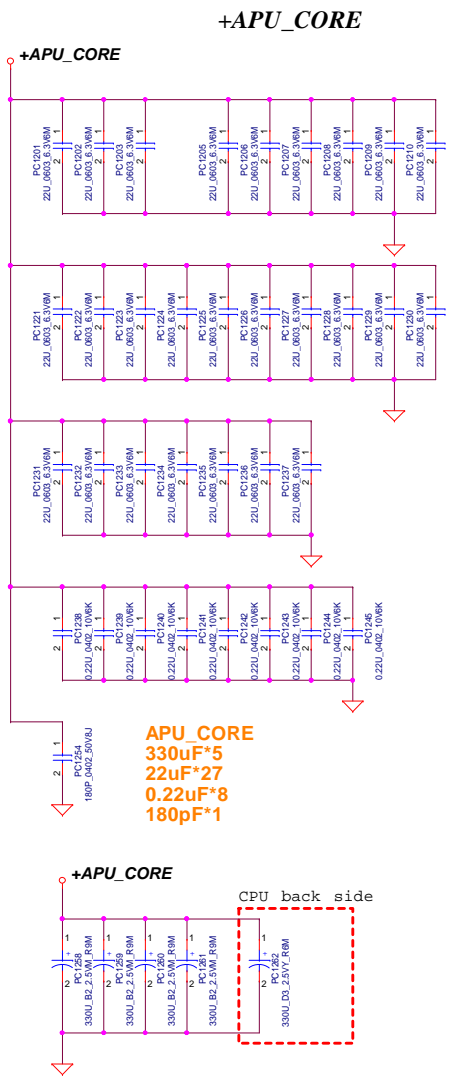
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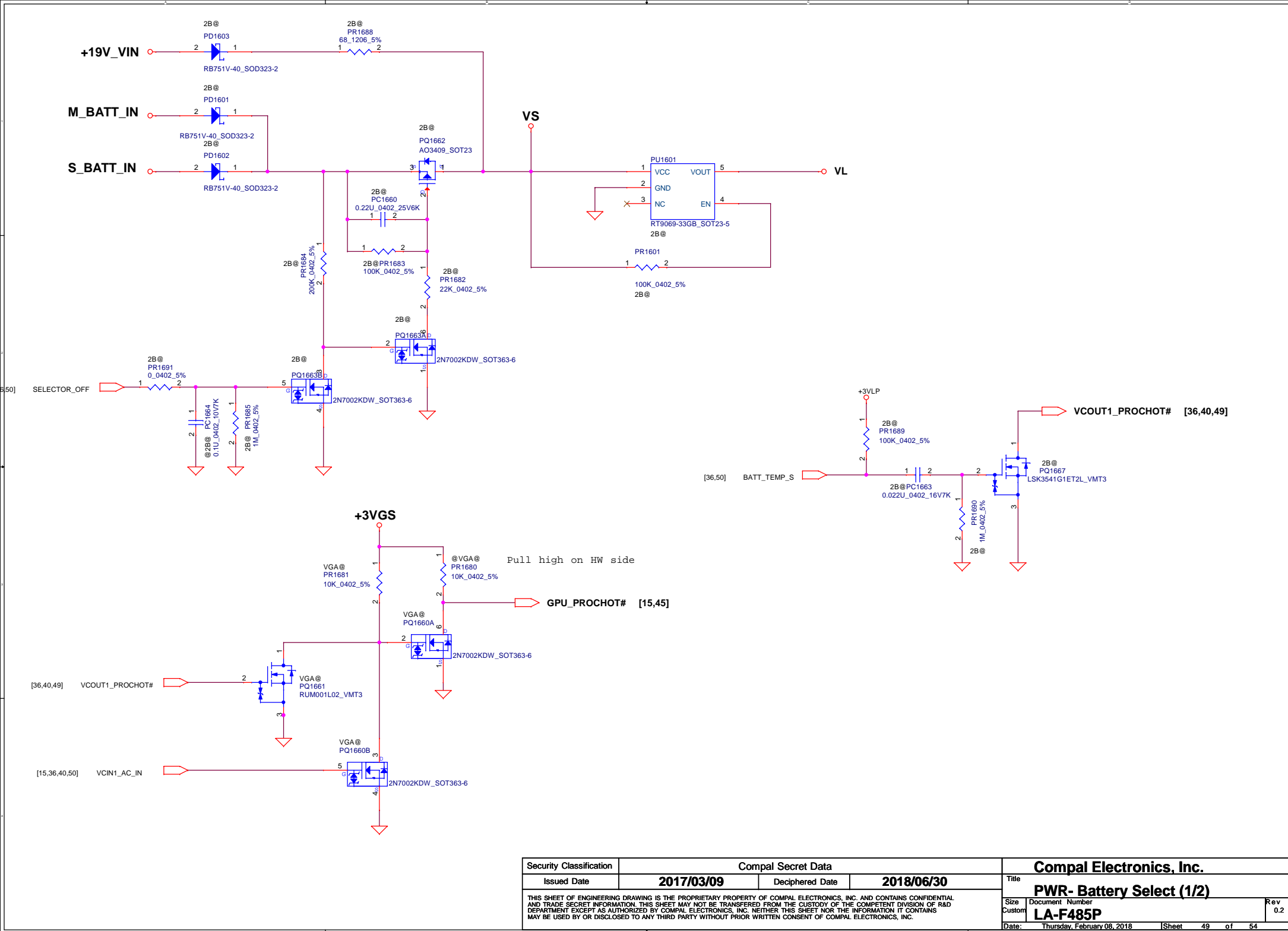
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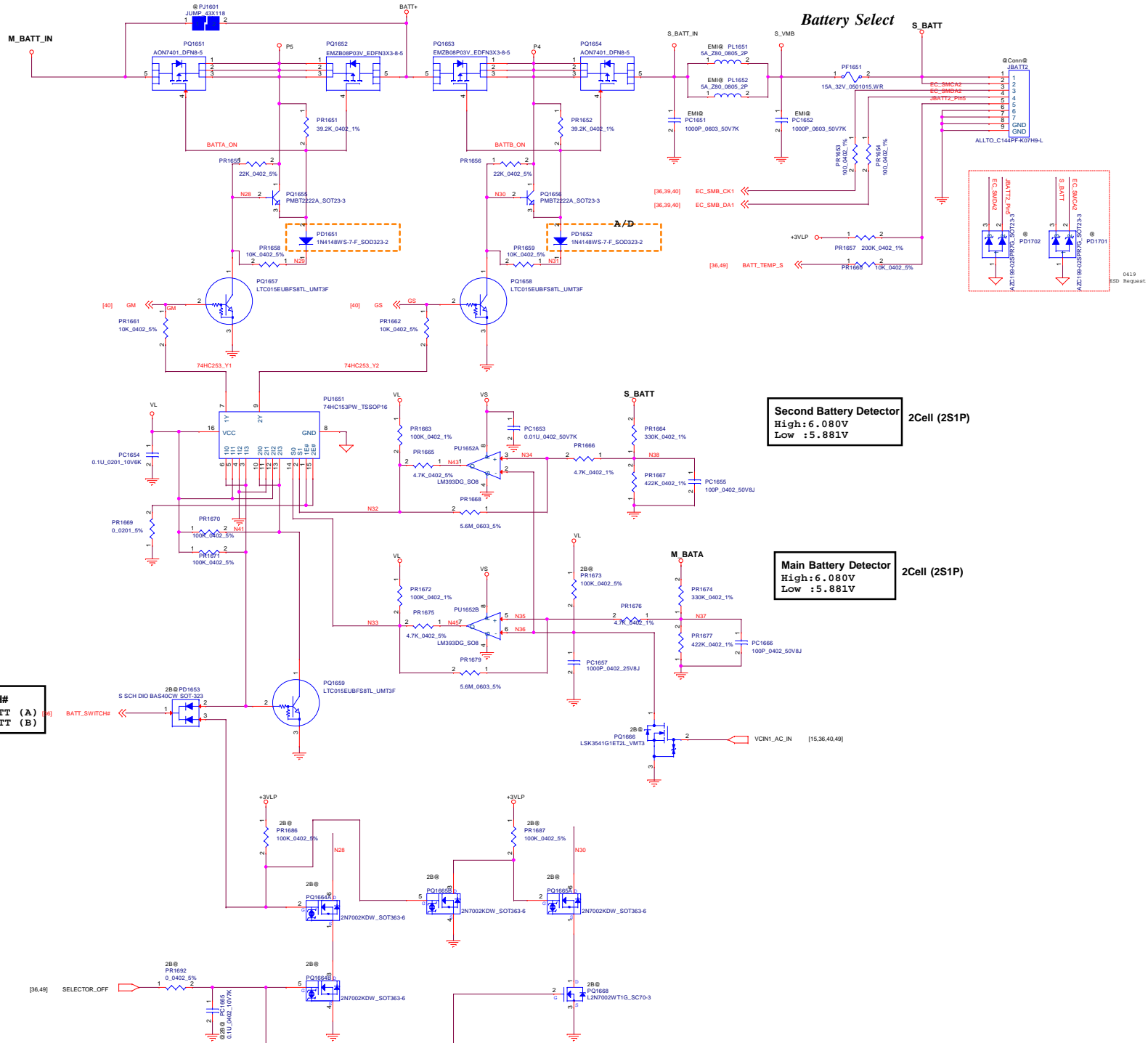
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**BATT\_SWITCH#**  
 High: M\_BATT (A)  
 Low : S\_BATT (B)

**Second Battery Detector**  
 High: 6.080V  
 Low : 5.881V

**Main Battery Detector**  
 High: 6.080V  
 Low : 5.881V

## Battery Select



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## Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Consider component de-rating		Change PF3 from SP040003U00(S FUSE 0438005.WR 5A 32V UL/CSA FAST) to SP040003Q00(S FUSE SI206-H-7.0A 7A 32V UL FAST)	6/23	EVT
2	To avoid acoustic issue		Change PC906,PC1004,PC1005,PC1017,PC1018,PC1037,PC1038,PC804,PC805 ,PC816,PC817 from SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE00000X200(S CER CAP 10U 25V M X5R 0603)	6/23	EVT
3	Change 5VLDO_EN to reserve		Add PR464(SD013000080,S RES 1/10W 0 +-5% 0603) Delete PQ455(SB00000VY00,S TR LSK3541G1ET2L 1N ) Delete PQ452(SB934130000,S TR AO3413 1P SOT-23 ) Delete PR462,PR463,PC463	6/23	EVT
4	To reduce VS LDO component		Delete PQ1601(SB00000VY00,S TR LSK3541G1ET2L 1N ) Delete PD1603(SCS00001200,S SCH DIO BAS40CW SOT-323 ) Delete PR1601,PR1602	6/23	EVT
5	Add remote sensing to +0.8VALW		Add PQ601(SB00000VY00,S TR LSK3541G1ET2L 1N ) Add PR618	6/23	EVT
6	Modify 2nd battery circuit		Change PD1601 from SC1N4148180(S DIO 1N4148WS-7-F SOD-323) to SCS00000Z00(S SCH DIO RB751V-40 SOD-323) Add PD1603(SCS00000Z00,S SCH DIO RB751V-40 SOD-323)	6/23	EVT
7	Modify APU_CORE & APU_CORE_SOC switching frequency from 300K to 400K		Change PR1015 & PR1016 to 0_0402_5% Change PR1018 to 69.8K_0402_1% Change PR1019 to 32.4K_0402_1%	6/23	EVT
8	Modify +0.8VALW OCP setting(min 9.5A)		Change PR612 to reserve	6/23	EVT
9	Modify BATGONE circuit		Change PR130 to 10K_0402_1% Add PC134 to 0.47U_0402_6.3V6K	6/23	EVT
10	Modify BATGONE circuit		Add PR135(0_0402_5%)	6/29	EVT
11	Modify +0.95VGS output voltage		Change PR1502 from 20K_0402_1% to 10K_0402_1%	6/29	EVT
12	Reduce S5 leakage current		Change PR413 from 47.5K to 475K Change PR414 from 10K to 100K	6/29	EVT
13	Remove PD function		Delete PC5,PC6,PC9,PD1,PQ1,PQ2,,PR1,PR2,PR3,PR5,PR6,PR7,PC12,PC13, PC14,PC15,PD3,PF3,PQ3,PQ4,PR16,PR17,PR18,PR19	6/29	EVT
14	Change charger IC solution to ISL88739A			6/29	EVT
15	Modify power sequence for GPU		Change PR902 from 0_0402_5% to 88.7K_0402_1% Change PR1503 from 0_0402_5% to 47K_0402_1% Add PC902 & PC1504(0.1U_0402_10V7K)	7/5	EVT
16	Change GPU CORE solution for R17M-P1-50 GPU		Change PU801 from RT3662EB to RT3662AC	7/25	EVT
17	Delete +0.95VGS power rail for GPU change		Delete PU1501	7/25	EVT
18	Change DDR power solution for cost saving		Change PU501 from SY8210AQVC to RT8207P	7/25	EVT
19	For reduce S5 leakage current , turn off selector in S5		Add PQ1662 ,PQ1663 Add PR1684 , PR1683 , PR1682, PR1691 , PR1685 Add PC1660 , PC1664	7/25	EVT
20	Add proshot function when 2nd battery removed		Add PQ1667 . PR1689 , PR1690 , PC1663	7/25	EVT
21	Modify 2nd battery circuit		Add PQ1666 , PQ1664 , PQ1665 , PD1653 Add PR1666 , PR1687 , PR1692	7/25	EVT
22	Modify for power sequence		Add PR613(100K_0402_5%)	8/8	EVT
23	Modify VGA CORE CHOKE and OCP setting		Change PL801,PL802 from 0.15UH +-20% 36A 7X7X4(SH00001EE00) to 0.15UH +-20% 35A 7X7X3(SH00001EF00) Change PR807,PR832 from 1.1K_0603_1% to 909_0603_1% Change PR816,PR843 from 1.1K_0402_1% to 909_0402_1% Change PR847 from 13K_0402_1% to 11.5K_0402_1% Change PR848 from 13.7K_0402_1% to 15K_0402_1% Change PR849 from 5K_0402_1% to 2.8K_0402_1%	8/9	EVT

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## Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modify 2nd battery circuit		Add PQ1668(L2N7002WT1G_SC70-3,SB00000ST00) Change PQ1662 from AO3413_SOT23-3 to AO3409_SOT23-3	9/26	DVT
2	Modify P/N for 2nd source		Change PD301 from SCS00008E00(LRB715FT1G SOT323-3) to SCS00001200(BAS40CW SOT-323)	9/26	DVT
3	Modify for AMD stardust test result		Change PR1046 from 80.6K_0402_1% to 100K_0402_1% Change PC1013 & PC1034 from 330P_0402_50V8J to 220P_0402_50V8J Change PR1027 from 24K to 33.2K	9/26	DVT
4	Correct BOM error		Add PR509(0_0402_5%) Delete PR1021(4.7K_0402_1%)	9/26	DVT
5	Modify for cost down action		Change PC1655 & PC1656 From SE068101K80(S CER CAP 100P 25V K NPO 0402) to SE071101J80(S CER CAP 100P 50V J NPO 0402)	10/6	DVT
6	Modify for cost down action(EMI)		Change PL1,PL2,PL3,PL4,PL1651 & PL1652 from SM01000P200(S SUPPRE_ 5A Z120 25M 0805) to SM01000U600(S SUPPRE_ 5A Z80 20M 0805)	10/6	DVT
7	Modify for cost down action(EMI)		Change PC315,PC413,PC428,PC517,PC605,PC903,PC1011,PC1027,PC1042 from SE025681K80(S CER CAP 680P 50V K X7R 0603) to SE074681K80 (S CER CAP 680P 50V K X7R 0402)	10/6	DVT
8	Follow AMD suggestion, modify 0.8VALWP to 0.9V		Change PR608 from 6.98K to 10K	10/16	DVT
9	Add remote sensing for 0.8VALWP		Add PR619, PR620 ,PR621(0_0402_5%)	10/16	DVT
10	Modify VR_HOT Setting		Change PR1019 from 32.4K_0402_1% to 316K_0402_1%	12/5	PVT
11	Change P/N		Change PC1006 & PC1007 SF000007200(common P/N) to SF000005200	12/5	PVT
12	Change P/N for shortage issue		Change PC313,PC314,PC426 SE000000U00(1U_0402_16V6K) to SE00000QL10 (1U_0402_10V6K)	12/5	PVT
13	Modify for GPU power sequence.		Add PR915(100K_0402_5%)	12/18	PVT
14	Modify cap for vendor's suggestion		Modify PC309 from 0.22U_0603_25V7K(SE000005Z80) to 0.47U_0603_16V7K(SE026474K80)	01/12	PreMP
15	Change to 0ohm short pad for part count reduce		Change PR312,PR316,PR319,PR334, ,PR401,PR410,PR504,PR509,PR513, PR601,PR607,PR609,PR619,PR620,PR621,PR812,PR813,PR814,PR834,PR835, PR836,PR840,PR831,PR837,PR839,PR901,PR1015,PR1016,PR1036,PR1037, PR1038,PR1032,PR1039,PR1041,PR1043 to 0ohm short pad	01/31	PreMP

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HW SVT PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	18/01/29	07	RC616, 617, 39, 19 change to short pad	Reduce part count
2	18/01/29	08	RC30, 35 change to short pad	Reduce part count
3	18/01/29	09	RC1672 change to short pad	Reduce part count
4	18/01/29	10	RC1676,1677,6126,6128,6129 change to short pad	Reduce part count
5	18/01/29	14	RV4 change to @	Follow GAE recommand
6	18/01/29	23	R6,10.463 change to short pad	Reduce part count
7	18/01/29	26	R43 change to short pad	Reduce part count
8	18/01/29	27	R3200 change to short pad	Reduce part count
9	18/01/29	28	R65,72,447,467 change to short pad	Reduce part count
10	18/01/29	30	R81,88,98,101,102 change to short pad	Reduce part count
11	18/01/29	31	R103,104,105 change to short pad	Reduce part count
12	18/01/29	32	R464 change to short pad	Reduce part count
13	18/01/29	33	R176/177 change to short pad	Reduce part count
14	18/01/29	36	R199/216/217 change to short pad	Reduce part count
15	18/02/01	26	R44~R47, R52 change to short pad	Reduce part count
16	18/02/02	9, 23	Delete DMIC_DET signal	For no used